RESEARCH PAPER
Contrib. Sci. & Tech Eng, 2024, 1(1)
Homepage: https://cste.journals.umz.ac.ir/
DOI: 10.22080/cste.2024.5008

Modeling MOSFET Threshold Voltage in TSMC 0.18um CMOS for Integrated Circuits Design

Amir Ebrahimi [1], Habib Adarang [2]*

[1] *School of Engineering, Royal Melbourne Institute of Technology (RMIT) University, Melbourne, VIC, Australia.*

[2] *Department of Electrical Engineering, Faculty of Engineering and Technology, University of Mazandaran, Babolsar. Iran.*

Article Info
Received 10 January 2024
Accepted 05 February 2024
Available online 15 March 2024

Keywords:
Threshold voltage (VTH);
Levenberg-Marquardt;
Short Channel Effect;
Drain-Induced Barrier Lowering (DIBL).

Abstract:
The threshold voltage of a MOSFET, represented by VTH, is a major parameter in the circuit design, and the lack of an accurate equation for the threshold voltage of transistors is one of the main challenges for integrated circuit designers. Based on the data obtained from the simulation, the present paper aims to investigate the effect of bias voltages (VGS, VDS, and VBS), transistor's dimensions (W and L), and temperature (T) on the value of threshold voltage, followed by the use of Levenberg-Marquardt method to propose a new equation for obtaining the threshold voltage value regarding different parameters. The obtained equation can be helpful for the design and manual calculations of the integrated circuits. Furthermore, various simulations were performed to evaluate the validity and accuracy of the obtained equation, indicating excellent consistency between the proposed equation and simulation results.

***Corresponding Author:** h.adarang@umz.ac.ir

Supplementary information: Supplementary information for this article is available at https://cste.journals.umz.ac.ir/

Please cite this paper as: Ebrahimi, A., & Adarang, H. (2024). Modeling MOSFET Threshold Voltage in TSMC 0.18um CMOS for Integrated Circuits Design. Contributions of Science and Technology for Engineering, 1(1), 1-11. doi: 10.22080/cste.2024.5008.

1. Introduction

A MOSFET's threshold voltage, represented by (V_{TH}), is a main parameter in the circuit design, which should be applied in modeling a transistor's behavior. Threshold voltage modeling is one of the most important requirements for a fairly accurate description of the transistor's electrical behavior. One of the major challenges of integrated circuit designers is the lack of an accurate equation for the transistor threshold voltage, by means of which the transistor's current can be calculated at high accuracy. Besides, in the ultra-low power design and sub-threshold region, it is necessary to apply the exact threshold voltage value of the transistor for the circuit design. Hence, various studies have proposed methods for measuring the threshold voltage or extracting an appropriate model in FETs (field-effect transistors) with high velocity and accuracy [1-3]. In Yu et al. [1], the advanced FVM (finite volume method) technique was applied to quickly measure the threshold voltage to obtain the MOSFET I-V characteristic. In Flandre et al. [4], the gm/Id method was used to determine the threshold voltage in MOSFET. In Agarwal et al. [5], the analytical model for MOSFET was improved so that it could be used to determine the quiescent point in SPICE. In de Jesus Costa et al. [6], the MOSFET model was attempted to improve to be used in manual calculations by investigating the dependence of threshold voltage on channel length. Chanda et al. [7] focused on modeling the MOSFET current in the sub-threshold region and expressed the dependence of threshold voltage on V_{BS} and V_{DS} voltages.

Additionally, temperature is another highly important parameter that strongly affects the transistor's behavior and, as a result, the circuit. In many circuits, to strengthen the circuit behavior relative to temperature, as in the voltage regulators or amplifiers, it is important to properly predict the threshold voltage behavior regarding temperature so that an appropriate temperature compensation method can be proposed [8 and 10]. Accordingly, Gupta and Kranti [11] focused on a more scrutinized investigation of the threshold voltage behavior regarding temperature. In this regard, some references have addressed the extraction of an equation for threshold voltage based on the physical concepts [12 and 13]. The analyses provided in these references depended on the physical parameters of the semiconductor and metal, including Fermi potential (ϕ_F), oxide capacitance (C_{ox}), metal-to-semiconductor work function difference (ϕ_B), and other parameters, which are commonly unavailable, leading consequently to the impossibility of the manual calculations for design.

In a standard CMOS process, the integrated circuit designers deal with the transistor's bias voltages (V_{GS}, V_{DS},

*ISSN **3060-6578***

and VBS) as well as its dimensions, namely W and L. Although the designer must be aware of the effect of different parameters on threshold voltage, a major problem in design is the lack of an equation with suitable accuracy for threshold voltage. Unfortunately, the currently existing equations governing the threshold voltage, which are found in various references, either lack sufficient accuracy or depend on the physical parameters of the semiconductor, complicating their application for manual calculations. This is why integrated circuit designers are not commonly interested in using such equations and usually attempt to obtain their intended characteristics through various simulations and even the trial and error method. However, such an approach would be time-consuming and increase the design complexities in many cases; therefore, one of the major requirements in this regard is to provide a more comprehensive model for the threshold voltage.

Considering the above-mentioned points, the threshold voltage value is one of the fundamental challenges in designing the integrated circuits, which is significantly affected, in general, by the parameters of bias voltages (V_{GS}, V_{DS}, and V_{BS}), dimensions of the transistor W and L, as well as temperature (T). As its principal objective, the present paper aims at mathematical modeling and obtaining an equation for threshold voltage based on the data derived from the simulations. In this work, modeling was performed using the Levenberg-Marquardt for curve fitting. The obtained equation can help design integrated circuits. The 0.18um CMOS TSMC process is widely used among integrated circuit designers; thus, the present paper addresses the modeling of threshold voltage in this type of technology.

The rest of this paper is organized as follows: section 2 investigates the factors affecting the voltage threshold so that they can be used in mathematical modeling. Section 3 explains the reduction of the short-channel effect in today's modern technology. Then, in section 4, the application of the Levenberg-Marquardt method for mathematical modeling is described, which will then be used to model the threshold voltage in the present paper.

In section 5, the effect of each of the parameters, including transistor width (W), drain-source voltage (V_{DS}), channel length (L), bulk-source voltage (V_{BS}), and temperature (T) on threshold voltage is simulated in TSMC CMOS 0.18um technology, leading to the presentation of the complete model of voltage threshold in section 6. The accuracy of the proposed model is also evaluated in this section. Finally, the conclusion is provided in section 7.

2. Factors Affecting Threshold Voltage

2.1. Short Channel Effects on Threshold Voltage

In an MOS transistor, as the channel length is reduced, the width of the depletion region in the drain-source junctions will become comparable to the channel length. In this case, various effects will alter the MOSFET function, known as short-channel effects [14]. Two of the different short-channel effects influence the threshold voltage, which will be discussed below.

2.1.1. Effect of Drain-Induced Barrier Lowering (DIBL) on Threshold Voltage

In a MOSFET, ideally, the channel current should be controlled by the gate voltage; however, as the channel length is reduced, the drain voltage will also affect the channel current due to the short drain-source distance. In fact, in a long-channel MOSFET, any change in the drain-source voltage will only affect the drain region, while with the reduction in the channel length, the drain voltage (V_D) will cause a lowering of the potential barrier between the source and channel. The potential barrier lowering is equivalent to the threshold voltage reduction, meaning that the voltage required to induce the source-to-drain electron flow will be reduced. This phenomenon is known as the effect of drain-induced barrier-lowering effect, the intensity of which will be increased with an increase in the drain voltage. This effect is shown in Figure 1, where the full line indicates the drain and source energy band in the equilibrium state, and the dashed line represents the same band in case of applied drain voltage along with the DIBL effect.

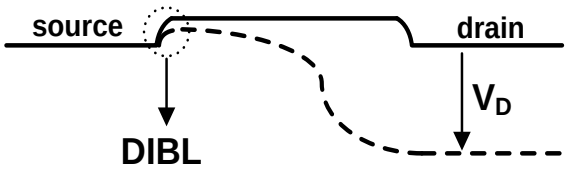
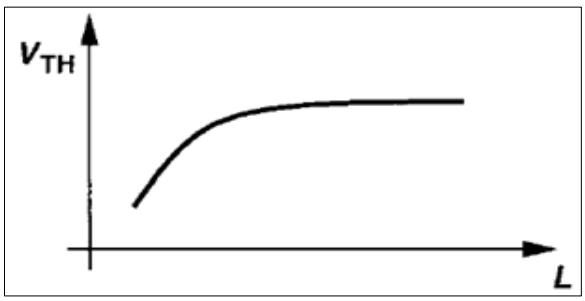


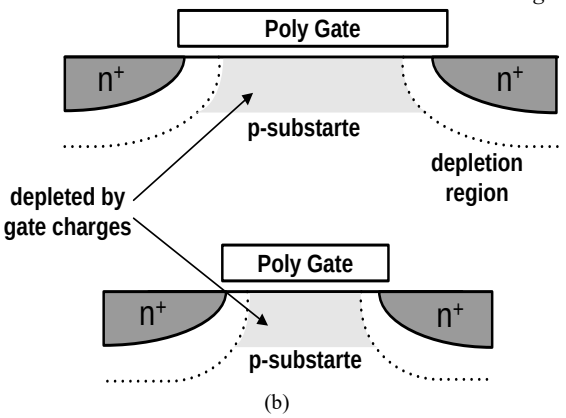
Figure 1. Drain-source energy band in equilibrium state and in case of applied drain voltage

2.1.2. Effect of Channel Length on Threshold Voltage

A phenomenon that appears with the shrinkage of the transistor is the dependence of threshold voltage on channel length. As shown in Figure 2-a, in a long-channel transistor, the threshold voltage value is rather constant and unchanged, but a transistor with a small L will exhibit lower V_{TH} with a reduction in the channel length because when the channel length is reduced, effective volume under the gate and between the drain and source empty regions will be decreased as well. Therefore, the formation of the inversion layer will require drainage of fewer charges from the substrate; as a result, the voltage required to be applied to the gate to form the inversion layer will also be reduced. This is demonstrated in Figure 2-b.



(a)



(b)

Figure 2. (a) Dependence of threshold voltage on channel length; (b) status of the inversion layer in case of short- and long-channel modes

2.2. Effect of Temperature on Threshold Voltage

In an MOS transistor, the voltage threshold depends on the temperature, which is reduced with an increase in the temperature. It is important to investigate the temperature dependence threshold voltage, particularly in applications such as voltage references; the temperature compensation is performed based on the threshold voltage behavior with temperature [14].

2.3. Effect of V_{SB} on Threshold Voltage

The threshold voltage of a MOSFET is influenced by the voltage difference between the source and bulk, referred to as the body effect. In an nMOS transistor, since the source (n +) - bulk (p +) junction is located in the reverse bias, the increased source voltage leads to the increased source-side empty region (between the channel and substrate), and consequently, the increased amount of charge required for the formation of the inversion layer. Therefore, in order for the inversion layer to be formed under the gate, a larger voltage should be applied to the gate. The following equation represents the effect of voltage V_{BS} on threshold voltage [14]:

$$V_{TH} = V_{TH0} + \gamma[\sqrt{2\varphi_S + V_{SB}} - \sqrt{2\varphi_S}] \quad (1)$$

where, ϕ_S and γ are transistor characteristics, which represent the surface potential and body effect coefficient, respectively. Also, V_{TH0} is the value of threshold voltage regardless of the body effect, and for V_{SB}=0, the value is positive in nMOS and negative in pMOS. As can be inferred from the above equation, the increased V_{SB} in a nMOS transistor yields a larger positive value for threshold voltage. However, in a pMOS transistor, since the threshold voltage has a negative value, an increase in the V_{SB} value results in a larger negative value for the threshold voltage, which is equivalent to the size reduction.

3. Reduction of Short Channel Effect

In modern processes, high-doping regions near the source and drain, known as ***halo*** or ***packet implementation***, reduce the short-channel effect. The halo regions cause a non-uniform doping rate along the channel. In fact, the doping concentration of the channel near the source and drain is higher than the one at its center. The presence of such regions incurs considerable elimination of the short-channel effect, just as the case for DIBL. However, in contrast to the short-channel effect wherein the threshold voltage decreased with a reduction in the channel length, as described in section 2.2, in devices with halo or packet implementation, the reduced channel length led to the increased V_{TH} value, which is known as reverse short-channel effect (RSCE). However, for long channels, the value threshold voltage approaches a constant and channel length-independent value. This behavior is represented in Figure 3.

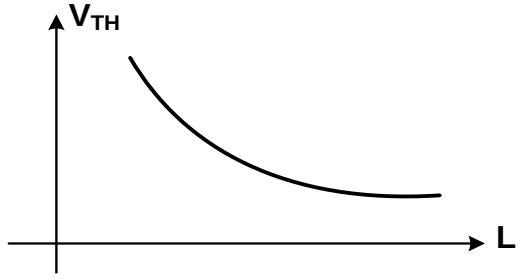


Figure 3. Dependence of threshold voltage on channel length in devices with halo implementation

4. Levenberg-Marquardt Method for Modeling

Since the present paper aims to mathematically model threshold voltage based on the data obtained from the simulation results, the Levenberg-Marquardt mathematical modeling method, which is used for curve fitting, has been explained in the appendix section. The ***cftool*** toolbox is used to apply this modeling method in MATLAB software.

5. Simulation and Modeling

In this section, using ADS software and in TSMC CMOS 0.18um technology, the effect of each of the parameters, including transistor width (W), drain-source voltage ($_{VDS}$), channel length (L), source-bulk voltage (V_{SB}), and temperature (T) on threshold voltage is simulated and studied in order to provide an appropriate mathematical model based on the Levenberg-Marquardt method as well as to predict the effect of each parameter on threshold voltage with high accuracy.

5.1. Simulation and Modeling of the Effect of VDS on Threshold Voltage

In order to investigate the effect of V_{DS} variations on threshold voltage, a transistor was biased, as in Figure 4. For the given channel length (L), the value of V_{DS} was changed from 50mV to 0.7V with 50mV steps, and for each V_{DS} value, the threshold voltage value was obtained through simulation and in ADS software. The curve for threshold voltage versus V_{DS} can be obtained by connecting these points. This method was performed along various channels, as shown in Figure 5. As can be seen, except for the small channel length L=0.2µm wherein the threshold voltage is very slightly dependent on V_{DS}, in the transistors with larger channel lengths, the increase in V_{DS} had no significant effect on the threshold voltage, which was due to the presence of

halo doping in modern technology. Therefore, the threshold voltage can be considered independent from V_{DS}. The independence of the threshold voltage from V_{DS} simplifies designing at various V_{DS} values.

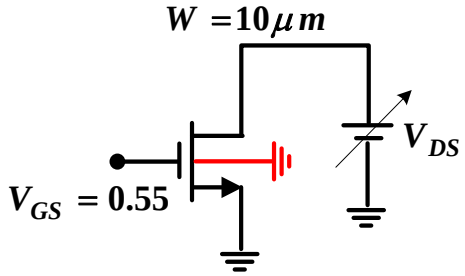


Figure 4. The bias of the nMOS transistor for simulating the effect of VDS variations on threshold voltage

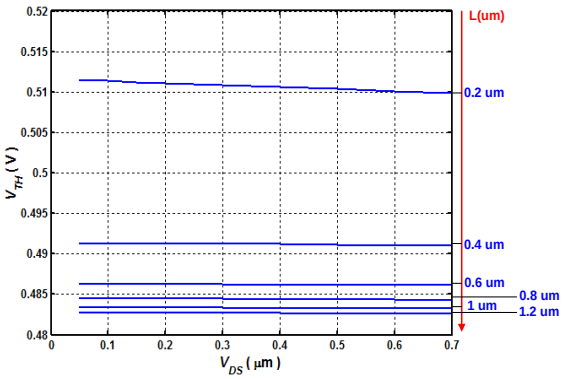


Figure 5. Effect of V_{DS} on threshold voltage value along different channels

5.2. Simulation and Modeling of the Effect of W on Threshold Voltage

An nMOS transistor was biased in order to investigate this effect, as shown in Figure 6. To prevent the effect of drain voltage (V_D) on threshold voltage, it was assigned a small value equal to 50mV. For the given channel length (L), the value of W was changed from 1μm to 30μm with 1μm steps, and for each W value, the threshold voltage value was obtained through simulation in ADS software. The curve for threshold voltage versus W can be obtained by connecting these points. This method was performed for three different channel lengths (0.3 μm, 0.5 μm, and 0.8 μm), yielding finally three V_{TH}-W curves, which are depicted in Figure 7.

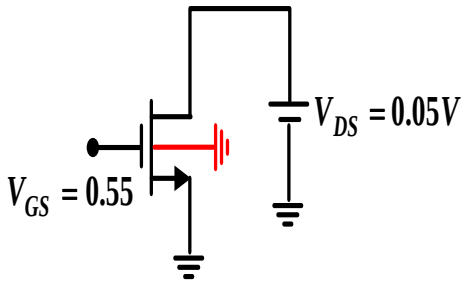


Figure 6. The bias of the nMOS transistor for simulating the effect of W variations on threshold voltage

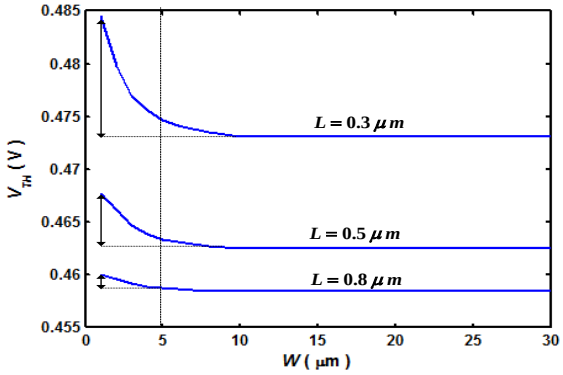


Figure 7. Dependence of threshold voltage on transistor width (W)

As in Figure 7, the threshold voltage variations relative to the W value are reduced with the increased channel length. On the other hand, the threshold voltage variations occur at small transistor widths (W); in other words, for W>5μm, the voltage threshold value will be approximately independent of the W size. Since in designing the integrated circuits, on the one hand, W>>L and, on the other hand, the minimum value is rarely used for L [14], the threshold voltage can be considered independent from W.

5.3. Modeling the Effect of L on Threshold Voltage

This section analyzes the effect of channel length on threshold voltage in both types of transistors, namely nMOS and pMOS. To investigate this effect, the nMOS and pMOS transistors were biased similarly as in Figure 8; i.e., for both transistor types, $|V_{DS}|$=0.05V, $|V_{GS}|$=0.55V, and V_{SB}=0 (without body effect). Furthermore, to ensure the independence of threshold voltage from W, the transistor width was selected equal to 10μm.

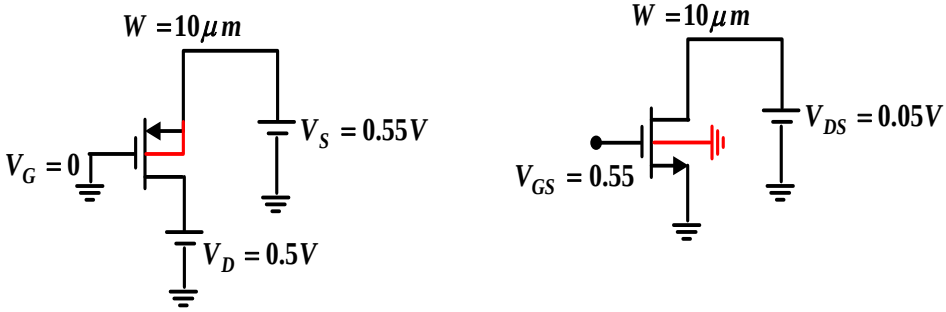


Figure 8. The bias of transistors for simulating the effect of L variations on threshold voltage

The value of L was changed from 0.2µm to 1.2µm with 0.05µm steps, and the threshold voltage value was obtained through simulation in ADS software for each value of L. The curve for threshold voltage versus L can be obtained by connecting these points, shown for both nMOS and pMOS transistors in Figure 9. It should be noted that the real value of the pMOS transistors' threshold voltage is negative, but the threshold voltage magnitude, i.e., the positive value, is depicted in Figure 9.

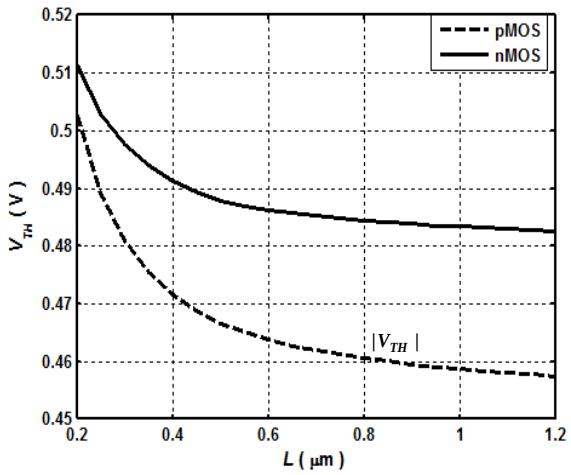


Figure 9. Curves for threshold voltage versus L for various types of transistor

The aim of modeling by the Levenberg-Marquardt method is to obtain an equation through which the threshold voltage behavior can be predicted with a minimum error rate. The threshold voltage behavior relative to L was considered as follows:

$$V_{TH}(L) = V_{TH0}[1 + f(L)] \quad (2)$$

where, V_{TH0} in 0.18µm technologies for nMOS and pMOS transistors is equal to 0.45V and -0.45V, respectively [14]. f(L) is a function of L that describes the threshold voltage variations relative to L and is obtained using the Levenberg-Marquardt method. In order for Equation 2 to properly describe the threshold voltage behavior relative to L, regarding Figure 9, f(L) was considered as follows:

$$f(L) = aL^b + c \quad (3)$$

The objective is to obtain the parameters a, b, and c for nMOS and pMOS transistors separately to match Equation 2 with the data obtained from the simulation, the curves of which are depicted in Figure 9. The ***cftool*** toolbox in MATLAB software was used to apply the Levenberg-Marquardt method. The results derived from this method, namely the intended parameters along with the root-mean-square error (RMSE), are represented in Table 1. Figure 10 depicts the V_{TH}-L voltage diagram that is simulated and modeled using Equation 2. A comparison between the simulated and modeled voltage threshold values based on Equation 2 indicates good consistency between the simulation and modeling results, as well as the accuracy of the equation obtained from the Levenberg-Marquard method.

Table 1. Equation (3)-simulation data matching parameters

	a	b	c	RMSE
nMOS	5.76×10^{-3}	-1.52	6.8×10^{-2}	1.72×10^{-4}
pMOS	10.4×10^{-3}	-1.46	9×10^{-3}	1.08×10^{-4}

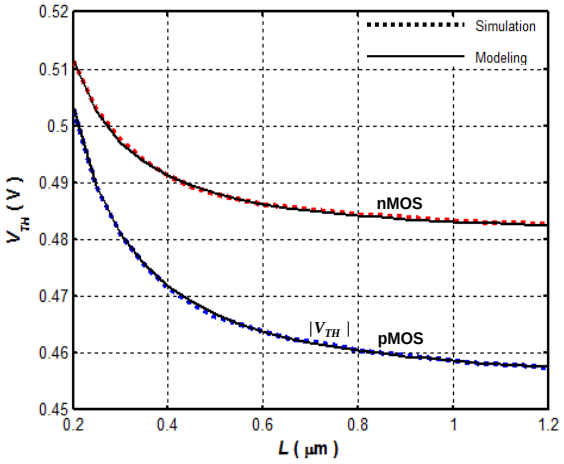


Figure 10. Curves for V_{TH} - L simulation and modeling results for nMOS and pMOS transistors

5.4. Modeling the effect of V_{SB} on Threshold Voltage

In this section, the effect of V_{SB} on threshold voltage in both nMOS and pMOS transistors is analyzed. To investigate this effect, the nMOS and pMOS transistors were biased, as in Figure 11, in which the values of bias voltages are also included. Moreover, in order for the independence of the threshold voltage from W, the value of the transistor width was selected equal to 10µm.

To investigate the body effect on threshold voltage, the value of V_{SB} was changed from 0V to 0.3V with 0.05V steps, and for each V_{SB} value, the threshold voltage value was obtained through simulation in ADS software. The curve for threshold voltage versus V_{SB} can be obtained by connecting these points, which is shown for both nMOS and pMOS transistors in Figure 12. To increase the modeling accuracy, the simulations were performed for different channel lengths ranging from L=0.2µm to L=0.5µm. It is emphasized that, for pMOS transistors with a negative threshold voltage, the absolute value of threshold voltage ($|V_{TH}|$) regarding V_{SB} is depicted in Figure 12-b. As can be observed, with an increase in V_{SB} value in an nMOS transistor, the threshold voltage will increase with a relatively constant gradient, while in a pMOS transistor, the threshold voltage value will decrease with a relatively constant gradient. This is a method used in low-voltage circuits to reduce the transistor's threshold voltage and, as a result, reduce the V_{GS} required for the transistor. Consequently, the supply voltage can also be reduced, which will ultimately lead to reduced power consumption.

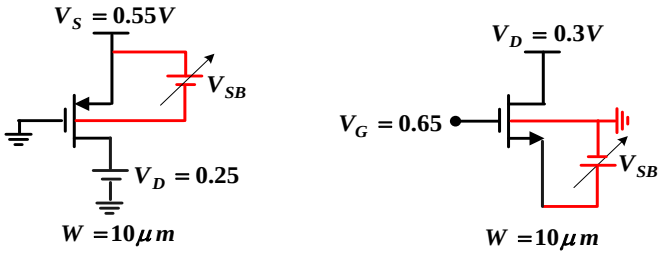
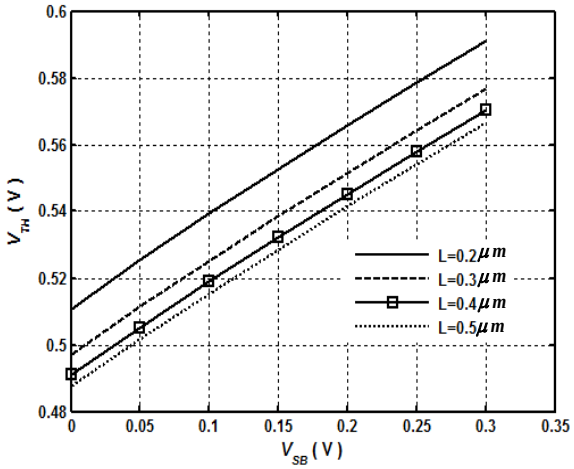
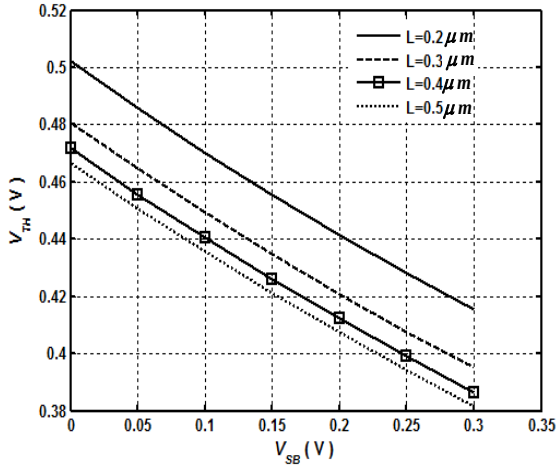


Figure 11. **The bias of transistors for simulating the effect of V_{SB} variations on threshold voltage**



(a)



(b)

Figure 12. **Simulation curves for threshold voltage versus VSB (a) for nMOS (b) for pMOS**

In order to model, it is necessary to obtain an equation that can predict the threshold voltage behavior regarding V_{SB} with a minimum error rate. The equation for the threshold voltage relative to V_{SB} was considered as follows:

$$V_{TH} = V_{TH}(L)[1 + g(V_{SB})] \quad (4)$$

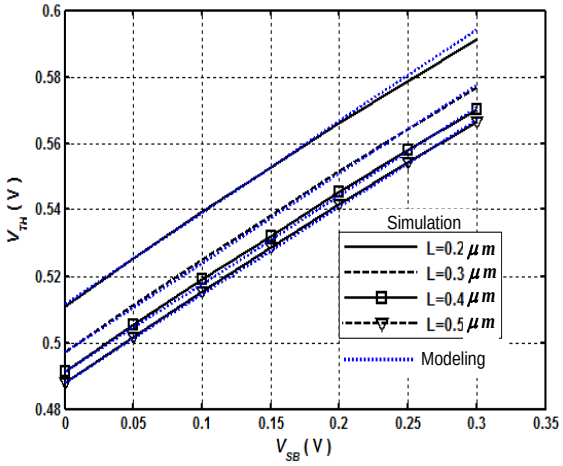
where $V_{TH}(L)$ is the value of threshold voltage for a given L, which is obtained from Equation 3. Also, $g(V_{SB})$ is a function of V_{SB} describing the threshold voltage variations with V_{SB}, which can be obtained from the Levenberg-Marquardt method. In order for Equation 4 to properly describe the V_{TH}-V_{SB} behavior and with regard to Figure 12 and the linear behavior of the curve, $g(V_{SB})$ was considered as follows

$$g(V_{SB}) = \beta V_{SB} \quad (5)$$

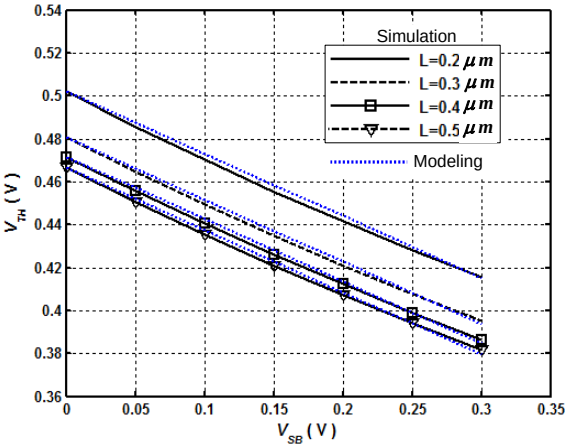
The purpose is to obtain the parameter β for nMOS and pMOS transistors separately in order for Equation 4 to match the data obtained from the simulation results, the curves of which are depicted in Figure 12. Results of the use of the Levenberg-Marquardt method, along with the RMSE, are presented in Table 2. Figure 13 depicts the V_{TH}-V_{SB} diagram simulated and modeled through Equation 4 for different channel lengths. A comparison between threshold voltage values simulated and modeled based on Equation 4 indicates good consistency between these results, representing the accuracy of the equation.

Table 2. **Equation (4)-simulation data matching parameters**

	β	RMSE
nMOS	0.54	0.8×10^{-3}
pMOS	-0.59	1.4×10^{-3}



(a)



(b)

Figure 13. Curves for VTH – VSB simulation and modeling results (a) for nMOS (b) for pMOS

5.5. Modeling the Effect of Temperature on Threshold Voltage

In order to investigate the effect of temperature (T) on threshold voltage, the nMOS and pMOS transistors were biased as in Figure 14 and values of the bias voltages are provided in this figure as well. Furthermore, the simulation was performed in case of V_{SB}=0, i.e. without body effect.

In order to investigate the effect of temperature (T) on threshold voltage and increase the modeling accuracy, a wide temperature range from -20˚C to +85˚C with +5˚C steps was considered and, for each temperature value, the threshold voltage value was obtained through simulation in ADS software. The threshold voltage curve versus T can be obtained by connecting these points, which is depicted in Figure 15 for nMOS and pMOS transistors and for different channel lengths.

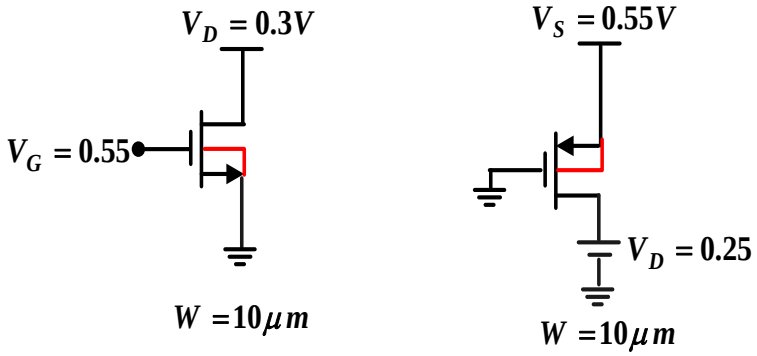


Figure 14. The bias of transistors for simulating the effect of temperature variations on threshold voltage (a) for nMOS (b) for pMOS

It is also emphasized that in this case as well, the absolute value of threshold voltage ($|V_{TH}|$) regarding V_{SB} is depicted in Figure 16-b for the pMOS transistor. As can be seen, increased temperature in both nMOS and pMOS transistors would lead to a reduction with a relatively constant gradient in threshold voltage.

Performing the modeling requires obtaining an equation that can predict the threshold voltage behavior relative to T with a minimum error rate. The equation of voltage threshold regarding T was considered as follows:

$$V_{TH} = V_{TH}(L)[1 + h(T)] \quad (6)$$

where, V_{TH} is the threshold voltage value at a given L, which can be obtained from Equation 2. Also, h(T) is a function of T describing the threshold voltage variations with temperature, which can be obtained from the Levenberg-Marquardt method. In order for Equation 6 to properly describe the V_{TH}-T behavior and with regard to Figure 15 and the linear behavior of the curve, h(T) was considered as follows:

$$h(T) = \alpha(T - T_0) \quad (7)$$

where, T_0 is the typical simulation temperature equaling +25˚C. The purpose is to obtain parameter α for the nMOS and pMOS transistors separately in order for Equation 6 to match the data derived from the simulation results. Furthermore, the root-mean-square error (RMSE) is also given in Table 3. It should be noted that, in Equation α presented in Table 3, the value of $V_{TH}(L)|_{T=T0}$ is obtained from Equation 2. Figure 16 depicts the V_{TH} - T diagram simulated and modeled using Equation 6. In order to achieve the desirable accuracy, the threshold voltage curve slope was analyzed at different channel lengths within an appropriate temperature range. A comparison between the threshold voltage values simulated and modeled based on Equation 6 indicates good consistency between these results, representing the accuracy of the obtained equation.

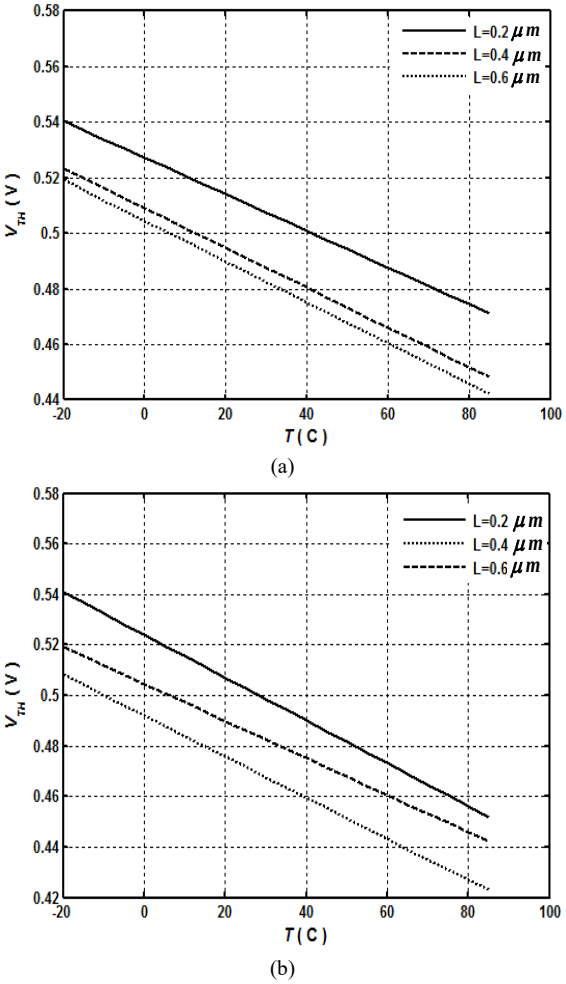
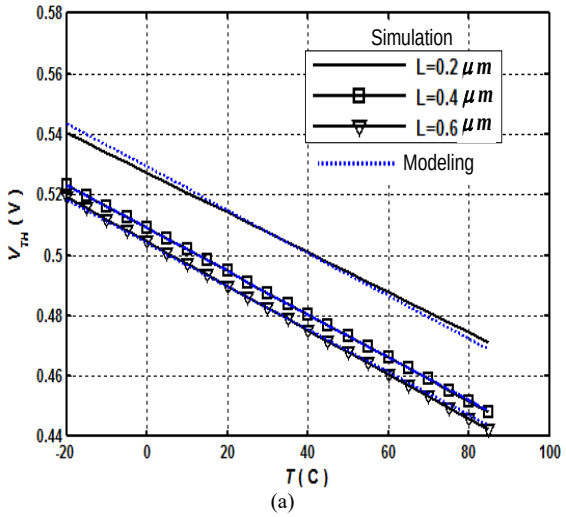


Figure 15. **Threshold voltage simulation curves versus temperature (a) for nMOS (b) for pMOS**

Table 3. **Equation (6)-simulation data matching parameters**

	α	RMSE
nMOS	$-\frac{0.68\times10^{-3}}{V_{TH}(L)\|_{T=T_0}}$	2.78×10^{-5}
pMOS	$-\frac{0.90\times10^{-3}}{V_{TH}(L)\|_{T=T_0}}$	3.22×10^{-5}



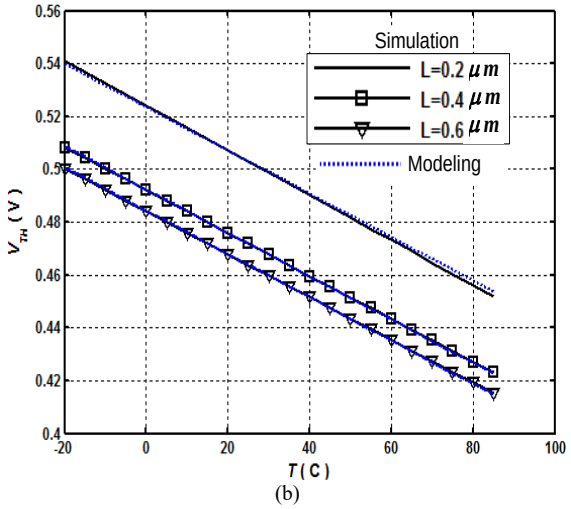


Figure 16. **V_{TH}-T simulation and modeling curves: (a) for nMOS (b) for pMOS**

6. Completed Model of Threshold Voltage

Considering all the points discussed in previous sections and regarding the models and simulations performed in section 1.5, the final and complete equation for threshold voltage per L, V_{SB}, and T in TSMC 0.18um CMOS technology is expressed as follows:

$$V_{TH} = V_{TH0}(1 + aL^b + c)(1 + \beta V_{SB})[1 + \alpha(T - 25)] \quad (8)$$

where a, b, c, α, and β are obtained in the simulation section for both nMOS and pMOS transistors. In Equation 8, the first and second terms are related to modeling the effect of channel length and body effect, and the third term is used to take the temperature effect into account. According to the explanations provided in section 5.2, the effect of the transistor width was ignored. On the other hand, due to halo doping, the TSMC 0.18um CMOS technology had a very insignificant DIBL effect, which was ignored in Equation 8.

Moreover, for further evaluation of the modeling, the simulations were performed for different values of temperature, L, and V_{SB}. The comparison between the threshold voltage value calculated from the modeling by Equation 8 and the values simulated for different values of the transistor parameters is represented in Figure 17. In these simulations, the temperature was increased from -20° C to +80° C, while other parameters were kept constant. Also, using the same method, V_{SB} and channel length (L) were increased from 0.1V to 0.5V and from 0.1µm to 1µm, respectively.

The results indicated good accuracy of the proposed modeling, so that it can provide a desirable understanding of the transistor's threshold voltage behavior.

7. Conclusion

In the present paper, based on the data derived from the simulations, the effects of bias voltages and transistor dimensions, along with temperature on the threshold voltage value, were investigated. Then, using Levenberg-Marquardt, a new equation was proposed to obtain the

threshold voltage value so that it could match the simulation data. The proposed equation had two major advantages. First, it indicated the dependence of the threshold voltage on effective parameters and could calculate the threshold voltage value with high accuracy. Second, the obtained equation can help with design as well as manual calculations regarding the integrated circuits. According to the tables and figures provided, it is obvious that the results of the present work can help the designer with circuit-level design.

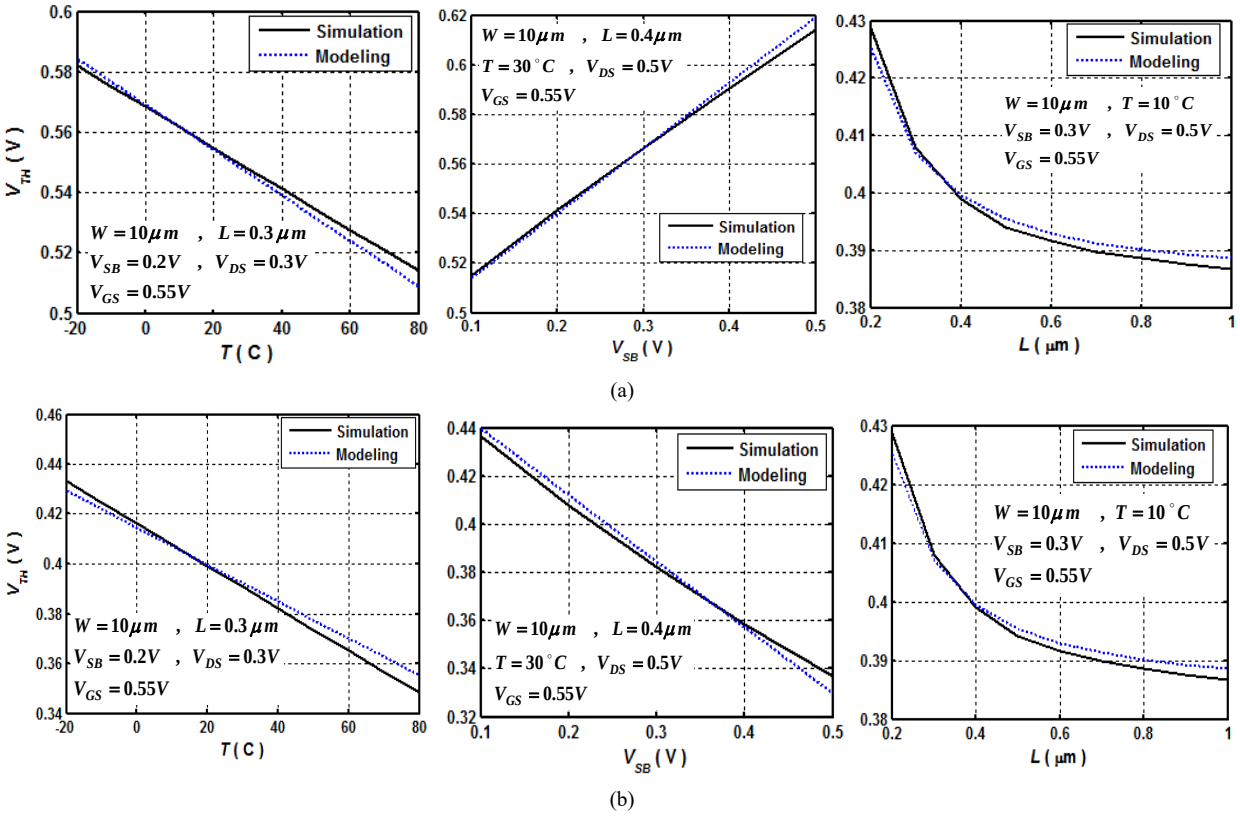


Figure 17. Comparison between simulation and modeling results for variations of different transistor parameters (a) nMOS (b) pMOS

8. References

[1] Yu, X., Cheng, R., Liu, W., Qu, Y., Han, J., Chen, B., Lu, J., & Zhao, Y. (2018). A Fast Vth Measurement (FVM) Technique for NBTI Behavior Characterization. IEEE Electron Device Letters, 39(2), 172–175. doi:10.1109/LED.2017.2781243.

[2] Luo, T. C., Chao, M. C. T., Tseng, H. C., Goto, M., Fisher, P. A., Chang, Y. Y., Chang, C. M., Takao, T., Iwasaki, K., & Lee, C. M. (2014). Fast transistor threshold voltage measurement method for high-speed, high-accuracy advanced process characterization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 22(5), 1138–1149. doi:10.1109/TVLSI.2013.2265299.

[3] Siebel, O. F., Schneider, M. C., & Galup-Montoro, C. (2012). MOSFET threshold voltage: Definition, extraction, and some applications. Microelectronics Journal, 43(5), 329–336. doi:10.1016/j.mejo.2012.01.004.

[4] Flandre, D., Kilchytska, V., & Rudenko, T. (2010). GmId method for threshold voltage extraction applicable in advanced MOSFETs with nonlinear behavior above threshold. IEEE Electron Device Letters, 31(9), 930–932. doi:10.1109/LED.2010.2055829.

[5] Agarwal, H., Gupta, C., Kushwaha, P., Yadav, C., Duarte, J. P., Khandelwal, S., Hu, C., & Chauhan, Y. S. (2015). Analytical modeling and experimental validation of threshold voltage in BSIM6 MOSFET model. IEEE Journal of the Electron Devices Society, 3(3), 240–243. doi:10.1109/JEDS.2015.2415584.

[6] de Jesus Costa, A., Alves, B. J., de Santana Soares, S., Santana, E. P., & Cunha, A. I. A. (2017). Improving a MOSFET model for design by hand. 2017 IEEE 8th Latin American Symposium on Circuits & Systems (LASCAS). doi:10.1109/lascas.2017.7948079.

[7] Chanda, M., Jain, S., De, S., & Sarkar, C. K. (2015). Implementation of Subthreshold Adiabatic Logic for Ultralow-Power Application. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 23(12), 2782–2790. doi:10.1109/TVLSI.2014.2385817.

[8] Zhang, Y., & Yuan, J. S. (2012). CMOS transistor amplifier temperature compensation: Modeling and analysis. IEEE Transactions on Device and Materials Reliability, 12(2), 376–381. doi:10.1109/TDMR.2011.2180388.

[9] De Oliveira, A. C., Cordova, D., Klimach, H., & Bampi, S. (2017). Picowatt, 0.45-0.6 v Self-Biased Subthreshold CMOS Voltage Reference. IEEE Transactions on Circuits and

Systems I: Regular Papers, 64(12), 3036–3046. doi:10.1109/TCSI.2017.2754644.

[10] Luong, P., Christoffersen, C., Rossi-Aicardi, C., & Dualibe, C. (2017). Nanopower, Sub-1 V, CMOS Voltage References with Digitally-Trimmable Temperature Coefficients. IEEE Transactions on Circuits and Systems I: Regular Papers, 64(4), 787–798. doi:10.1109/TCSI.2016.2632072.

[11] Gupta, M., & Kranti, A. (2017). Variation of Threshold Voltage with Temperature in Impact Ionization-Induced Steep Switching Si and Ge Junctionless MOSFETs. IEEE Transactions on Electron Devices, 64(5), 2061–2066. doi:10.1109/TED.2017.2679218.

[12] Fasarakis, N., Karatsori, T., Tassis, D. H., Theodorou, C. G., Andrieu, F., Faynot, O., Ghibaudo, G., & Dimitriadis, C. A. (2014). Analytical modeling of threshold voltage and interface ideality factor of nanoscale ultrathin body and buried oxide SOI MOSFETs with back gate control. IEEE Transactions on Electron Devices, 61(4), 969–975. doi:10.1109/TED.2014.2306015.

[13] Mezzomo, C. M., Bajolet, A., Cathignol, A., Di Frenza, R., & Ghibaudo, G. (2011). Characterization and modeling of transistor variability in advanced CMOS technologies. IEEE Transactions on Electron Devices, 58(8), 2235–2248. doi:10.1109/TED.2011.2141140.

[14] Johns, D. A., & Martin, K. (2008). Analog integrated circuit design. John Wiley & Sons, Hoboken, United States.

Appendix A

A.1. Model Selection

Modeling or system identification is a hot topic in all engineering fields. There are many methods for modeling a system, which include neural networks, fuzzy sets, genetic programming, genetic algorithm and gradient based methods. Model selection basically consists of two basic parts; structure selection, and parameter optimization. The structure of a model may be heuristic or mathematical or even a combination of both.

Parameter optimization is the next step that determines the validity of the model. Parameter optimization methods are divided into two main categories: random search algorithms and gradient-based algorithms. There are a variety of random search algorithms that are updated every day and include genetic algorithm (GA), particle swarm optimization (PSO), simulated annealing (SA), ant colony (AC), and so on. The second category in parameter optimization belongs to gradient-based methods, which are also used in this research. They include methods that utilize the first derivative or gradient of the model, like steepest descent, or the second derivative, like Newton's method, or the approximation of them, like quasi-Newton's method. In the sequel, the least square method and Levenberg-Marquardt (LM) method are described, respectively.

A.2. Least-square Method for Parameter Identification

In the least-square (LS) method, the mean square of the error between the model output and the system output is minimized by modifying the parameters of the model. The mathematical formulation of the method is as follows. Suppose that the system is affine in parameters, i.e., it could be written in regression form:

$$y(i) = \sum_{j=1}^{n} \phi_j(i)\theta_j^* = \phi^T(i)\theta^* \quad \text{(A-1)}$$

where θ^* is the original unknown parameter of the system, and $\varphi^T(i)$ is the vector of the known part of the system, e.g., the former input and outputs of the system. The goal is to estimate θ^* so that the cost function V (θ,t) is minimized. If we define $\hat{\theta}$ as the estimate of θ^*, we would have:

$$\hat{y}(i) = \sum_{j=1}^{n} \phi_j(i)\hat{\theta}_j = \phi^T(i)\hat{\theta} \quad \text{(A-2)}$$

$$\varepsilon(i) = y(i) - \hat{y}(i) = y(i) - \phi^T(i)\theta \quad \text{(A-3)}$$

$$Y(t) = [y(1)y(2)\dots y(t)]^T \quad \text{(A-4)}$$

$$E(t) = [\varepsilon(1)\varepsilon(2)\dots\varepsilon(t)]^T \quad \text{(A-5)}$$

$$\varphi(t) = \begin{bmatrix} \phi^T(1) \\ . \\ . \\ \phi^T(t) \end{bmatrix} \quad \text{(A-6)}$$

$$V(\theta,t) = \frac{1}{2}\sum_{i=1}^{t} \varepsilon^2(i) = \frac{1}{2}E^TE = \frac{1}{2}||E||^2 \quad \text{(A-7)}$$

$$2V(\theta,t) = E^TE = (y-\varphi\theta)^T(y-\varphi\theta) = y^T.y - y^T\varphi\theta - \theta^T\varphi^Ty + \theta^T\varphi^T\varphi\theta \quad \text{(A-8)}$$

By taking the derivative of $V(\theta,t)$ with respect to $\hat{\theta}$ and setting the result to zero, the answer which minimizes the cost function is achieved as follows:

$$\hat{\theta} = (\varphi^T\varphi)^{-1}\varphi^Ty \quad \text{(A-9)}$$

The LS response is consistent in affine models. In other words, the estimated parameters converge to original parameters as the number of observations increases. On the other hand the unbiased convergence of the LS method is not guaranteed in non-affine models. This issue opens the field of nonlinear optimization to the discussion.

A.3. Levenberg–Marquardt nonlinear least-square algorithm

As mentioned in the model selection section, there are a variety of methods in nonlinear model identification. One of the reputed methods in gradient-based parameter identification is the LM method, which uses the approximation of hessian matrix in the calculation of a minimum. This method converges to the local minimum and is dependent on the initial guess in finding the local minimum. The algorithm, in short, is as follows. Suppose that the input-output pair (x,y) is approximated by a nonlinear function $f(x,\hat{\theta})$:

$$\hat{y} = f(x,\hat{\theta}) \quad \text{(A-10)}$$

The cost function $V(\hat{\theta},x)$ is defined as (.). If we expand the Taylor series of the function $f(x,\hat{\theta})$ around a point $(x_0,\hat{\theta}_0)$ we have:

$$f(x,\hat{\theta}+\delta) \approx f(x,\hat{\theta}) + J\delta \quad \text{(A-11)}$$

where, $J = \frac{f(x,\hat{\theta})}{\partial\hat{\theta}}$ is the Jacobian vector of f with respect to parameters$\hat{\theta}$. If the approximate A-11 is substituted in the cost function $V(\hat{\theta}, x)$ results:

$$V(\hat{\theta}+\delta,x) = \sum_{i=1}^{n}(y_i - f(x_i,\hat{\theta}) + J_i\delta)^2 = ||Y - F(x,\hat{\theta}) - J\delta||^2 = [Y - F(x,\hat{\theta})]^T[Y - F(x,\hat{\theta})] - 2[Y - F(x,\hat{\theta})]^T J\delta + \delta^T J^T J\delta \quad \text{(A-12)}$$

By taking the derivative of $V(\hat{\theta}+\delta,x)$ with respect to δ and setting the result to zero, the optimum variation in parameters in each iteration yields as:

$$(J^T J)\delta = J^T[Y - F(x,\hat{\theta})] \quad \text{(A-13)}$$

$$\delta = (J^T J)^{-1} J^T[Y - F(x,\hat{\theta})] \quad \text{(A-14)}$$

A fault of the above solution is that the Jacobian vanishes near the minimum, and the inverse would be ill-posed. To pave this issue, Levenberg proposed the addition of a damping factor λ as follows:

$$\delta = (J^T J + \lambda I)^{-1} J^T[Y - F(x,\hat{\theta})] \quad \text{(A-15)}$$

This remedy has the shortcoming that if the parameter λ is large, the effect of $J^T J$ in the inversion would be neglected. As a result, Marquardt proposed the addition of scaling in each component of the gradient according to its curvature. As a result, I would be replaced with $diag(J^T J)$. In this way, there would be larger movement along the directions where the gradient is smaller. This avoids slow convergence in the direction of a small gradient. The final formula for the variation of parameters in each iteration would be as follows:

$$\delta = [J^T J + \lambda diag(J^T J)]^{-1} J^T[Y - F(x,\hat{\theta})] \quad \text{(A-16)}$$

This algorithm is provided in the curve-fitting toolbox of the MATLAB which makes the use of the algorithm so easy.