



A Low-Noise SiGe:C HBT Amplifier with Novel Input Matching Technique for Bluetooth Applications

Sedighe Babaei Sedaghat ^{1*}, Mortaza Mojarad ¹, Fatemeh Zadehparizi ²

¹ Assistant professor, Department of Electrical and Computer Engineering, Urmia University, Urmia, Iran.

² Assistant professor, Department of Electrical Engineering, Jahrom University, Jahrom, Iran.

Article Info

Received 01 July 2025
Accepted 27 October 2025
Available online 26 May 2026

Keywords:

Low Noise Amplifier (LNA);
SiGe:C BiCMOS;
Heterojunction Bipolar Transistor (HBT);
Input Matching;
IHP SiGe:C HBT;
Bluetooth.

Abstract:

This paper presents a novel SiGe:C HBT low-noise amplifier (LNA) architecture, specifically designed to cover the Bluetooth band (2.402–2.4835 GHz) within a wider operational range of 2.2–2.65 GHz. The proposed design introduces an innovative L–C ladder matching technique that generates left-half-plane (LHP) zeros, effectively canceling the poles and achieving a flat impedance response across a wide frequency range. This approach not only enhances input matching but also contributes to a lower noise figure (NF) by suppressing transistor thermal noise at the output node. Additionally, a new biasing network for the cascode stage is implemented to improve S_{11} and NF simultaneously, demonstrating strong compatibility with the 0.13 μm SiGe:C BiCMOS process. Simulation results show that the proposed LNA achieves a maximum gain of 23 dB, NF of 2.2 dB, and IIP₃ of +14.45 dBm, while consuming only 40 mW from a 3.3 V supply. The LNA maintains stable performance across a 450 MHz bandwidth (2.2–2.65 GHz), resulting in a Figure of Merit (FOM) of 19.2, which outperforms comparable state-of-the-art designs. Owing to its innovative matching and biasing networks, the proposed structure achieves high linearity, excellent gain, and low noise, making it a promising front-end solution for next-generation Bluetooth and low-power wireless communication systems).

© 2026 University of Mazandaran

*Corresponding Author: s.babaeisedaghat@urmia.ac.ir

Supplementary information: Supplementary information for this article is available at <https://cste.journals.umz.ac.ir/>

Please cite this paper as: BabaeiSedaghat, S., Mojarad, M., & Zadehparizi, F. (2026). A Low-Noise SiGe:C HBT Amplifier with Novel Input Matching Technique for Bluetooth Applications. Contributions of Science and Technology for Engineering, 3(2), 29-37. doi:10.22080/cste.2025.29586.1062.

1. Introduction

The microwave frequency spectrum, typically covering 1–30 GHz, offers a compact wavelength and high data rate capability, making it attractive for modern short-range wireless standards such as Bluetooth [1]. For wireless applications, Silicon Germanium (SiGe) is an excellent semiconductor technology. It provides high-frequency and high-speed performance required for wireless systems. Additionally, it enables RF and digital functions on a single integrated circuit (IC) [2].

It has been demonstrated that better noise behavior can be achieved in high frequencies for a transistor by adding carbon to the base of a SiGe HBT [3, 4]. Therefore, the SiGe:C HBT has emerged as a technology for RFICs owing to the maturity of the silicon process and its high performance [5]. Many integration issues that appear in SiGe:C BiCMOS technology are discussed by Laurens et al. [6].

Most earlier articles have focused on extracting transistor parameters from the hybrid-T equivalent circuit, with only

a limited number using the hybrid- π equivalent circuit. Although the physics of transistors is directly aligned with the hybrid-T model, the most widely used simulators—including HICUM, VBIC, SGP, and Agilent HBT—are based on the hybrid- π topology. As a result, extracting parameters for the hybrid- π HBT model has recently become more significant [7].

One of the most common RF bands is the 2.4-GHz. Hence, the need to design wireless transceivers operating in the 2.4 GHz band has prompted a comprehensive investigation of related system architectures and integrated-circuit designs [8]. Using radio waves instead of wires is one of the benefits of the Bluetooth standard. This wireless standard is prone to interference, because it catches low power signals. Therefore, an LNA with reduced NF is an essential component in the design of Bluetooth systems. The Bluetooth spectrum allocation is shown in Figure 1. LNA is a crucial block in high frequency front-end receivers, because it has an impressive effect on overall system noise performance [9–13]. It should be noted that numerous trade-offs exist among performance metrics, including impedance



matching, noise figure, gain, power consumption, and stability, in LNA design [14-16]. For wideband LNA design purposes, the principal goal is to attain desired input matching over the bandwidth of interest [17, 18].

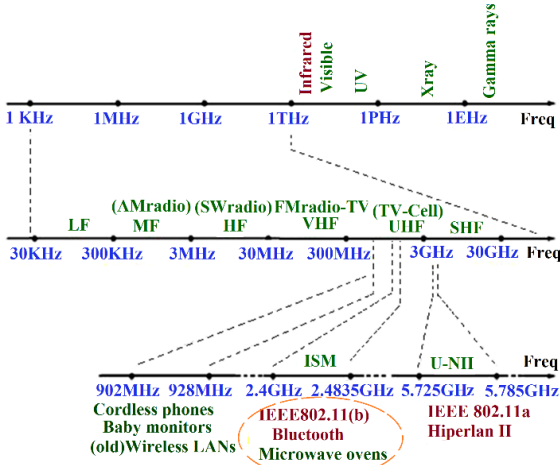


Figure 1. The Bluetooth spectrum allocation [9]

In this paper, by utilizing an accurate model of SiGe:C HBTs [19] and the newly proposed LC ladder technique to

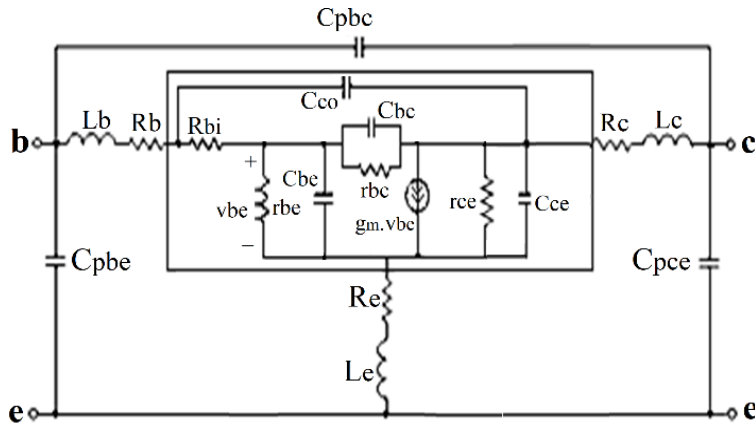


Figure 2. The hybrid-π equivalent circuit of SiGe:C HBT [19]

2.1. Definition of Y-Parameters

The use of Y-parameters is the most effective method for determining small-signal circuit parameters [7, 19, 20]. The bias dependent intrinsic parameters of the proposed transistor which are depicted in Figure 2, are obtained as follows:

$$C_{bc} = \frac{\text{imag}(Y_{i11} + Y_{i12})}{\omega} \quad (1)$$

$$R_{be} = \frac{1}{\text{real}(Y_{i11} + Y_{i12})} \quad (2)$$

$$C_{bc} = \frac{\text{imag}(Y_{i12})}{\omega} \quad (3)$$

$$R_{bc} = -\text{real}(Y_{i12}) \quad (4)$$

$$C_{ce} = \frac{\text{imag}(Y_{i12} + Y_{i22})}{\omega} \quad (5)$$

implement the matching networks, an LNA circuit with broadband input matching and improved noise figure for the Bluetooth standard is proposed. The structure of the paper is as follows. In Section 2, the characteristics of the SiGe:C HBT transistor are extracted for a hybrid-π equivalent circuit. The proposed LNA circuit is presented in Section 3. In Section 4, the circuit analysis, including input impedance and noise, is presented. In Section 5, the simulation results and a comparison with other recently reported works are presented. The conclusion is given in section 6.

2. De- Embedding and Extraction of Elements

In Figure 2, a small-signal equivalent circuit model in the forward active region for a SiGe:C transistor has been shown. The model used is the linearized version obtained from the well-known hybrid-π equivalent circuit [20]. Based on Figure 2, this circuit is divided into 2 sections: The bias-dependent intrinsic elements are located in the inner section, and most of the extrinsic elements, which are bias-independent, are located in the outer section. To obtain a more precise model, the analysis and the model include the intrinsic base resistance. To avoid accumulating errors, it is essential to include the base resistance.

$$R_{ce} = \frac{1}{\text{real}(Y_{i12} + Y_{i22})} \quad (6)$$

$$g_{m0} = \sqrt{[\text{real}(Y_{i21}) - \text{real}(Y_{i12})]^2 + [\text{imag}(Y_{i12}) - \text{imag}(Y_{i21})]^2} \quad (7)$$

$$\tau = \frac{\sin^{-1}\left(\frac{\text{imag}(Y_{i21} - Y_{i12})}{g_m}\right)}{\omega} \quad (8)$$

Where: $g_m = g_{m0}e^{-j\omega\tau}$, $\omega = 2\pi \times \text{freq}$

$$R_{bi} = \text{real}\left(\frac{1}{Y_{i11}}\right) \text{ at high frequency} \quad (9)$$

$$C_{co} = \text{imag} \frac{(Y_{i11} \times Y_{i22} - Y_{i12} \times Y_{i21})}{\omega (Y_{i11} + Y_{i21})} - C_{bc} \quad (10)$$

The input impedance is given in Equation 11, and all bias-dependent intrinsic elements have also been considered according to the proposed SiGe:C HBT transistor model.

$$Z_{in} = (R_b + R_{bi} + \frac{\alpha + \beta}{\gamma + \delta} \parallel \rho) \quad (11)$$

The bias-independent extrinsic parameters can be calculated using Equations 12 to 18. It is worth noting that, due to the complexity of the input impedance formula, certain parameters, such as α , β , δ , and ρ , are defined below for simplicity.

$$\alpha = (Z_e + Z_{be})(r_{ce}R_c + Z_{bc}R_c + r_{ce}Z_{bc}) \quad (12)$$

$$\beta = Z_e Z_{be}(R_c + r_{ce}Z_{bc}R_c g_m + r_{ce}Z_{bc}g_m + Z_{bc}) \quad (13)$$

$$\gamma = r_{ce}R_c + Z_{bc}R_c + r_{ce}Z_{bc} + Z_{be}R_c + r_{ce}Z_{be}R_c g_m \quad (14)$$

$$\delta = Z_e Z_{bc} + r_{ce}Z_e + r_{ce}Z_{be}Z_e g_m + r_{ce}Z_{be} + Z_{be}Z_e \quad (15)$$

$$\rho = \frac{1}{j\omega(C_{pbe} + C_{pbc})} \quad (16)$$

$$Z_{be} = R_{be} \parallel \frac{1}{j\omega C_{be}} \quad (17)$$

$$Z_{bc} = R_{bc} \parallel \frac{1}{j\omega C_{bc}} \quad (18)$$

where C_{bc} , C_{be} , and g_m are base-collector capacitance, base-emitter capacitance and the transconductance of the transistor (Q1) respectively. C_{pbc} and C_{pbe} are the base-collector and base-emitter parasitic capacitors, respectively. Also, R_c , R_b , and R_e denote the extrinsic collector, base, and emitter resistances, respectively. The input impedance can be determined readily using Equations 11 to 18; further details are provided by Karimi et al. [7], and Karimi and Banitalebi [19].

3. The Proposed LNA Structure

To show the high accuracy of the SiGe:C HBT model, a Low-Noise Amplifier (LNA) has been designed and implemented for Bluetooth applications. The schematic of the newly proposed LNA structure is shown in Figure 3. It consists of a transistor (Q1) which forms a common emitter (CE) amplifier and the transistor (Q2) is the cascode device, enhancing input-output isolation and bandwidth; input matching is primarily shaped by the L1-C1-RC network around Q1.

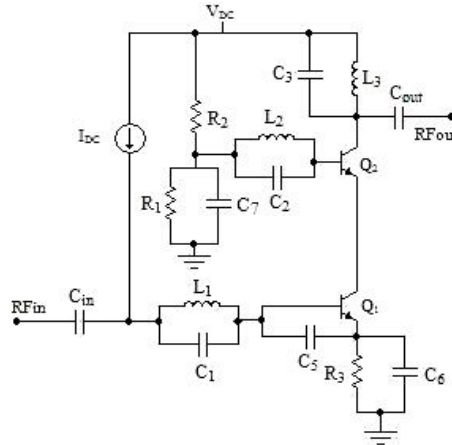


Figure 3. Schematic of the suggested structure for LNA

The LNA can be viewed as a combination of a CE amplifier, which acts as a transconductor, while the other transistor with the common base (CB) structure acts as a current buffer. The benefits of the cascode topology are its high gain and high reverse isolation. Moreover, its Miller effect is very small, thereby enhancing stability and enabling high-frequency operation.

The R-C circuit in the emitter of transistor Q1 is designed to improve input matching. The ladder L1-C1 is connected to the base of Q1 to improve the noise figure and achieve better input matching. The proposed matching network is designed to generate left-half-plane (LHP) zeros that cancel poles, yielding a flat impedance function over a broader frequency range. The capacitance C5 has been added between the base and emitter terminals of Q1, thereby improving the noise figure and stability. However, it decreases the power gain. To curtail this drawback, a good

balance between noise figure and power gain has been established with ($C5=0.01\text{pF}$).

The resonant circuit L2-C2 has been connected to the base of the transistor Q2 to improve the noise figure. When L2 increases, the stability deteriorates. Therefore, the value of inductance should be limited ($L2=1\text{nH}$, $C2=5.6\text{pF}$). The resonant circuit L3-C3 provides the DC bias for the transistors and acts as the LNA load. In the next section, the circuit analysis is elaborated in greater detail.

The main idea of this work is to use L-C tanks at the bases of Q1 and Q2 to reduce the noise figure, and to use an R-C circuit at the emitter of Q1 to improve input matching in the amplifier. Moreover, the transistor's thermal noise contribution is effectively suppressed at the output, thereby improving the noise figure. This has been verified through circuit analysis and extensive simulations.

4. Circuit Analysis

This work utilizes a modified cascode configuration. The circuit analysis is carried out by simplifying the proposed small-signal equivalent model.

4.1. Input Impedance Analysis

The transfer function of the input impedance of the proposed low-noise amplifier has been calculated according to the small-signal equivalent shown in Figure 4.

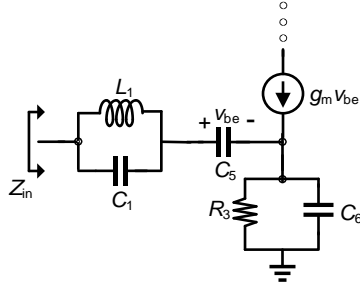


Figure 4. The small-signal equivalent circuit for input impedance calculation

To obtain a simplified expression for the input impedance, the common-emitter current gain (β) has been assumed to be very large, and the early effect has been ignored. The proposed matching network is designed to generate left-

half-plane (LHP) zeros to cancel poles, thereby achieving a flat impedance function over a wide frequency range. To investigate the efficacy of the newly presented technique, the poles and the zeros of the input impedance function have been obtained as follows:

$$\omega_{z1} = \frac{R_L}{L_1}, \omega_{z2} = \frac{1}{C_1 R_L}, \omega_{z3} = \frac{g_m C_1}{(C_1 C_5 + C_1 C_6 + C_5 C_6)} \quad (19)$$

$$\omega_{p1} = 0, \omega_{p2} = \frac{1}{R_3 C_6}, \omega_{p3} = \frac{R_L}{L_1}, \omega_{p4} = \frac{1}{C_1 R_L}$$

By inspecting the pole-zero locations above, it can be concluded that by choosing the zero frequency ω_{z3} much smaller than the pole frequency ω_{p2} , a design constraint can be approximately calculated and is given by:

$$g_{m1} \ll \frac{C_5 + C_6}{R_3 C_6} \quad (20)$$

As a result, the impedance reduction caused by the poles ω_{p3} and ω_{p4} is compensated by the impedance increment caused by ω_{z1} and ω_{z2} . Consequently, a flat magnitude for the impedance can be achieved over a wider frequency range, which can be given by $\omega_{p2} - \omega_{z3}$.

The magnitude of the input impedance of the proposed LNA has been conceptually depicted in Figure 5.

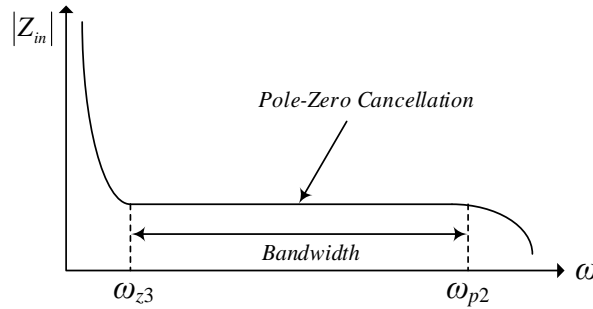


Figure 5. The conceptual input impedance magnitude function

4.2. Noise Analysis

One major characteristic of the proposed LNA structure is that the effect of the thermal noise of the transistor Q1 can

be nullified at the output of the circuit, leading to NF improvement. This can be demonstrated by considering the small-signal equivalent circuit for the noise analysis of Q1, as depicted in Figure 6.

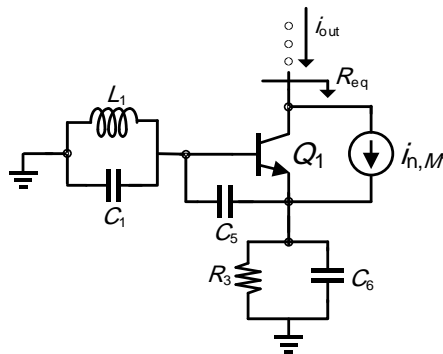


Figure 6. Noise Analysis for the transistor Q1

Based on Figure 6, and by assuming that C_5 , which is the base-emitter parasitic capacitance, is very small, which implies $C_1 \gg C_5$, the thermal noise transfer function has been calculated and is given by:

$$\frac{i_{out}}{i_{n,M1}} = \frac{C_6 C_5 R_1 R_3 s^2 + C_6 R_3 s + 1}{C_6 C_5 R R_3 s^2 + C_6 R_3 s + 1 - g_{m1} R_3} \quad (21)$$

Where R_1 is equal to $\omega \times Q \times L_1$ and Q is the quality factor of the LC tank formed by the inductor L_1 and the capacitor C_1 . By considering Equation 21, to minimize the magnitude of the transfer function, $g_{m1} R_3$ should be much smaller than unity ($g_{m1} R_3 \ll 1$). This is because the magnitude of the above transfer function at the resonant frequency ω_0 is obtained as follows:

$$\omega_0 = \frac{1}{\sqrt{C_6 R_3 C_5 R_1}}$$

$$\left| \frac{i_{out}}{i_{n,M1}} \right| = \frac{\omega_0 C_6 R_3}{\sqrt{(\omega_0 C_6 R_3)^2 + (1 - g_{m1} R_3)^2}} \quad (22)$$

It is deduced that for $g_{m1} R_3 \ll 1$, the magnitude of the transfer function in Equation 22 drops below unity, leading to better noise performance. Regarding the noise contribution of the transistor Q_2 , for a larger equivalent resistance R_{eq} shown in Figure 6, the noise transfer function is approximately equal to zero. Since the new bipolar transistor has a large Early voltage, R_{eq} is sufficiently large, and the effect of the thermal noise of Q_2 is quite negligible in the overall NF of the LNA. The dominant noise source is the thermal noise of the resistor R_3 . The transfer function for this thermal noise has also been calculated as follows:

$$\frac{i_{out}}{i_{n,R3}} = \frac{g_{m1} R_3}{C_6 C_5 R_1 R_3 s^2 + C_6 R_3 s + 1 + g_{m1} R_3} \quad (23)$$

As expressed above, $g_{m1} R_3$ should be smaller than unity, for which the magnitude of the noise transfer function in Equation 23 can also be given by

$$\left| \frac{i_{out}}{i_{n,R3}} \right| = \frac{g_{m1} R_3}{\sqrt{(\omega_0 C_6 R_3)^2 + 1}} \quad (24)$$

Considering the resonant frequency in Equation 22, the function in Equation 24 can be expressed as

$$\left| \frac{i_{out}}{i_{n,R3}} \right| = \frac{g_{m1} R_3}{\sqrt{\left(\frac{C_6 R_3}{C_5 R_1}\right)^2 + 1}} \quad (25)$$

Therefore, since $g_{m1} R_3 \ll 1$ and for the constraint derived in Equation 26, the noise contribution of R_3 becomes small, leading to better NF.

$$C_6 R_3 \ll C_5 R_1 \quad (26)$$

4.3. Linearity Analysis

The nonlinear behavior of the proposed amplifier can be described using the exponential relation between the collector current and the base-emitter voltage of transistor Q_1 :

$$i_c = I_s \left(e^{v_{BE}/V_T} - 1 \right) \quad (27)$$

Expanding the exponential term around the bias point gives the small-signal nonlinear model:

$$g_m v_{be} + \frac{g_m}{2V_T} v_{be}^2 + \frac{g_m}{6V_T^2} v_{be}^3 \quad (28)$$

Where $g_m = \frac{I_c}{V_T}$. The first term represents the linear transconductance, while the higher-order terms are responsible for harmonic and intermodulation distortion. For a two-tone input, these nonlinearities produce intermodulation components at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, which determine the amplifier's linearity. The input-referred third-order intercept point (IIP3) can be estimated from this model as $VIIP3 = V_T \cdot \sqrt[3]{8} \approx 2.83 V_T$, corresponding to approximately 74 mV at room temperature.

The emitter inductor L_1 introduces local negative feedback, thereby linearizing the transconductance. The emitter impedance $Z_E = j\omega L_1$ reduces the base-emitter voltage swing according to:

$$v_{be} = v_{in} / (1 + g_m \cdot Z_E) \quad (29)$$

Consequently, the effective nonlinear coefficients become:

$$a_{1,eff} = a_1 / (1 + g_m \cdot Z_E) \quad (30)$$

$$a_{3,eff} = a_3 / (1 + g_m \cdot Z_E)^3 \quad (31)$$

Because the ratio $a_{1,eff} / a_{3,eff}$ increases with $|Z_E|$, the circuit exhibits a higher IIP3 and thus improved linearity. This comes at the cost of a modest reduction in gain, typical of emitter-degenerated stages.

Moreover, the input matching network ($L_1 C_1 - C_{in}$) improves linearity by generating a real component of the input impedance at the operating frequency, thereby mitigating phase distortion and intermodulation distortion.

The cascode transistor Q_2 maintains a nearly constant collector voltage for Q_1 , suppressing variations in v_{CE1} and the associated modulation of the base width. This minimizes distortion in the collector current and significantly reduces third-order intermodulation components. In addition to enhancing linearity, the cascode topology increases input-output isolation and extends the amplifier's bandwidth.

The RC bias and LC feedback networks around the input stage stabilize the DC operating point and limit dynamic variations in v_{BE} . As a result, the collector current and transconductance remain nearly constant during large-signal operation, reducing higher-order derivatives such as $\partial^2 g_m / \partial v_{BE}^2$. This mechanism further suppresses harmonic generation and intermodulation products, thereby improving overall linearity without significant degradation in noise figure (NF).

Based on analytical estimates, the proposed linearization mechanism provides approximately 3–5 dB improvement in IIP3 compared with conventional cascode LNAs fabricated in the same HBT process.

5. Simulation Results

The proposed LNA circuit was simulated in the TT process corner at 27 °C using the Advanced Design System (ADS) software. The design is implemented in a 0.13 μm BiCMOS process using the RF SiGe:C HBT model from IHP and is intended for operation in the Bluetooth frequency band. Scattering parameters.

The simulation result for S21 is depicted in Figure 7. The proposed LNA exhibits a high and nearly flat power gain

across the intended frequency range. The gain remains above 23 dB from 2.4 to 2.65 GHz, and above 21.6 dB over the wider span of 2.2–2.65 GHz, demonstrating good broadband characteristics. The limited gain variation ($\approx \pm 0.8$ dB) across the passband validates the effectiveness of the proposed matching network and makes the circuit well-suited for Bluetooth receivers that require consistent amplification and minimal in-band ripple.

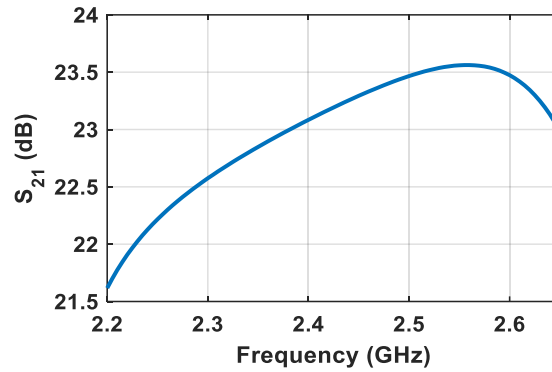


Figure 7. The power gain (S₂₁) of the suggested LNA

The simulated S-parameters of the proposed LNA are shown in Figure 8. As can be observed, the bandwidth is approximately equal to 450 MHz, and the simulated values

for S₁₁, S₁₂, and S₂₂ are -15 dB, -28 dB, and -10 dB, respectively.

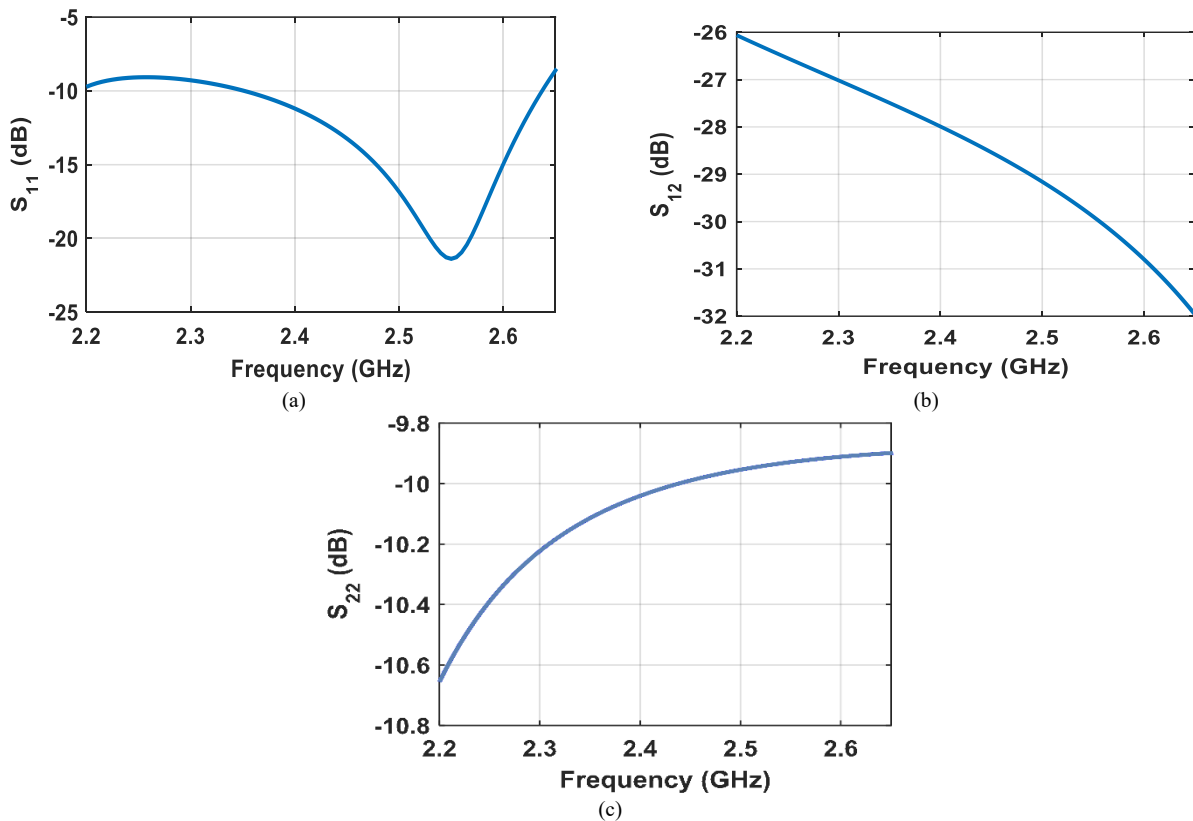


Figure 8. (a) The input reflection coefficient (S₁₁), (b) The reverse isolation (S₁₂), (c) output reflection coefficient (S₂₂), of the suggested LNA

5.1. Noise Performance

The noise figure is another fundamental performance parameter of LNAs. According to Friis equation in Equation

32, it is obvious that the LNA stage has the most contribution to the overall noise of the receiver [21]. It

should be noted that a receiver is a cascade of numerous building blocks such as LNA, filter, and Mixer.

$$NF_{total} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_1} + \dots + \frac{NF_n - 1}{A_1 \cdot A_{n-1}} \quad (32)$$

As it is implied from Equation 32, the noise of the frontend stages is of utmost importance regarding the overall noise Figure. In addition, for decreasing the noise contribution of the following stages, a high gain LNA is required as can be

deduced from Equation 27. In Figure 9 the simulated noise figure is shown, and it can be observed that the noise figure (NF) of the proposed LNA remains very low across the operating band, varying from approximately 2.1 dB to 3.0 dB within the 2.2–2.7 GHz range, which aligns well with the Bluetooth operating frequency around 2.4 GHz. This indicates effective input matching to the transistor’s optimum noise impedance and confirms the suitability of the design for low-noise Bluetooth front-end applications.

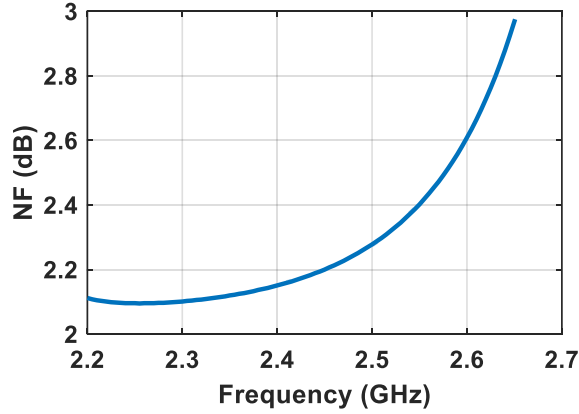


Figure 9. Noise Figure

5.2. Linearity

The linearity of the proposed LNA was evaluated through two-tone simulations around the 2.4 GHz Bluetooth band and the result is shown in Figure 10. With input tones of −40 dBm, the output spectrum exhibited a dynamic range of 108.9 dB between the fundamental and third-order

intermodulation components, leading to an IIP₃ of +14.5 dBm. This high intercept point verifies the amplifier’s strong linear response with negligible distortion, demonstrating an effective balance among gain, noise performance, and linearity—well-suited for Bluetooth low-power front-end applications.

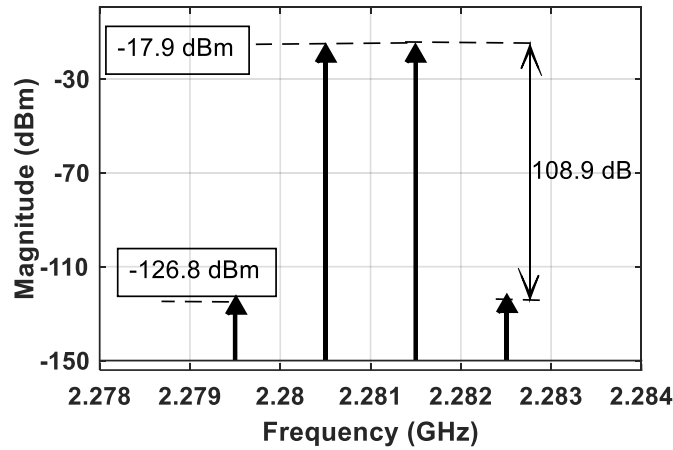


Figure 10. The linearity of the proposed LNA

5.3. Stability

In addition to the important parameters mentioned, stability is a critical consideration in LNA design. The μ stability factor was used to assess unconditional stability. Compared with the traditional K, Δ criteria, μ provides a more compact and robust indicator. The amplifier is considered stable for $\mu > 1$, which is satisfied throughout the operating frequency range. The μ -factor provides a continuous and unified measure of unconditional stability

derived directly from the S-parameters of the two-port network, and is defined as:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12} S_{21}|} \quad (33)$$

where $\Delta = S_{11} S_{22} - S_{12} S_{21}$. Based on the simulation results, the proposed LNA is unconditionally stable over the frequency range of 2.2 GHz to 2.65 GHz as shown in Figure 11.

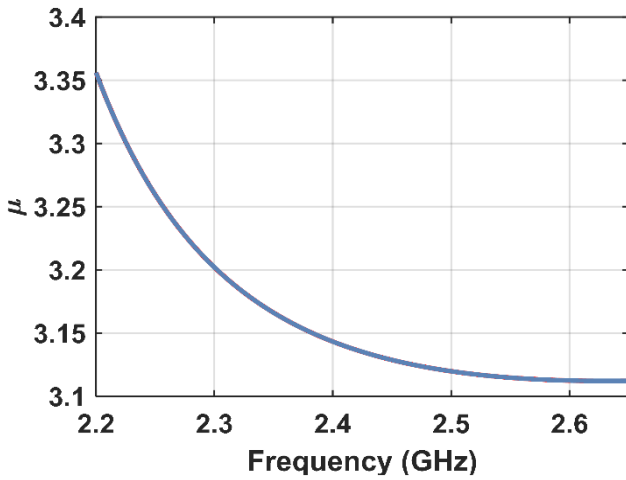


Figure 11. μ Factor indicating unconditional stability

5.4. Comparison

The performance of some recently reported low-noise amplifiers is compared with that in this work in Table 1. It has been shown that the proposed LNA has a good balance between noise figure, power gain, and input matching. To ensure a fair comparison among different LNA designs with varying performance specifications, a Figure of Merit (FOM) is defined to encompass the key performance parameters of the amplifier. The defined FOM is dimensionless and expressed as follows.

$$Fom = 10 \log \left(\frac{Gain(linear) \cdot IIP3(mW)}{P_{dc}(mW) \times NF(linear)} \right) \quad (34)$$

Table 1. Comparison of the Suggested LNA results with other works

Ref.	Freq.(GHz)	Nf (dB)	Power cons.(mW)	S21 (dB)	IIP3	FOM
Rahman and Harjani [23]	2.3	2.8	0.457	17.4	-10.7	7.3
Lee et al. [24]	2.4	4.51	0.3	13.96	-16.6	-2.27
Shirmohammadi and Yavari [25]	0.47-3.3	2.57	12.5	22	2.81	11.26
Snehitha Reddy and Nath [26]	2.4	3.8	25.41	17.9	-18.13	-18
Zhang et al. [27]	2.33-2.46	1.6	39.3	20.3	5	8.07
This work	2.2- 2.65	2.2	40	23	14.45	19.22

As shown in Table 1, although the circuit exhibits relatively high power consumption, its low noise figure, high gain, and strong linearity result in a favorable overall figure of merit (FOM) for the proposed LNA.

6. Conclusion

In this work, a low-voltage RF BiCMOS low-noise amplifier (LNA) employing a novel cascode configuration has been proposed for Bluetooth applications. The circuit is implemented in $0.13 \mu\text{m}$ IHP SiGe:C HBT BiCMOS technology based on the hybrid- π model. The innovative aspects of the design include using passive L-C networks to reduce the noise figure and an R-C emitter network in Q1 to improve input matching. The proposed matching concept introduces left-half-plane (LHP) zeros to counteract the poles, forming a flat impedance profile across a wider frequency range. This technique also mitigates the transistor's thermal noise, thereby lowering the overall noise figure. Simulation results confirm a maximum gain of 23 dB with 40 mW power consumption. The LNA achieves excellent linearity with an IIP₃ of +14.5 dBm, demonstrating strong resistance to intermodulation distortion. The calculated Figure of Merit (FOM) further validates the proposed design, demonstrating that despite moderate power consumption, the combination of high gain, low noise, and high linearity yields superior overall performance. Moreover, the amplifier maintains stable characteristics over a 450 MHz bandwidth (2.2–2.65 GHz), ensuring reliable operation across the entire Bluetooth and

adjacent ISM frequency bands. These results confirm that the proposed LNA offers an efficient and reliable front-end solution for Bluetooth and other low-power wireless communication systems.

7. References

- [1] Mohammadjany, A., Miar-Naimi, H. (2026). A High-Gain, Low CRR, Narrow Beam Width Enhanced Vivaldi Antenna for Through-the-Wall Imaging Radar. *Contrib. Sci. & Tech Eng*. 3(1). Doi:10.22080/cste.2025.29067.1035.
- [2] Nguyen, K. M. (2006). A 77GHz power amplifier in silicon germanium BiCMOS technology. PhD Thesis, Massachusetts Institute of Technology, Massachusetts, United States.
- [3] Winkler, W., Borngraeber, J., Heinemann, B., Herzel, F., & Scholz, R. (2004). High-frequency low-noise amplifiers and low-jitter oscillators in SiGe:C BiCMOS technology. *Noise in Devices and Circuits II*, 5470, 185. doi:10.1117/12.544513.
- [4] Bardin, J. C. (2009). Silicon-germanium heterojunction bipolar transistors for extremely low-noise applications. , PhD Thesis, California Institute of Technology, California, United States.
- [5] Haramé, D. L., Ahlgren, D. C., Coolbaugh, D. D., Dunn, J. S., Freeman, G. G., Gillis, J. D., Groves, R. A., Hendersen, G. N., Johnson, R. A., Joseph, A. J., Subbanna, S., Victor, A. M., Watson, K. M., Webster, C. S., & Zampardi, P. J. (2001).

- Current status and future trends of SiGe BiCMOS technology. *IEEE Transactions on Electron Devices*, 48(11), 2575–2594. doi:10.1109/16.960385.
- [6] Laurens, Martinet, Kermarrec, Campidelli, Deleglise, Dutarte, ... & Monroy. (2003). A 150GHz $f_{sub T}/f_{sub max}/0.13/spl mu/m$ SiGe: C BiCMOS technology. 2003 Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting, IEEE, 28-30 September, 2003, Toulouse, France.
- [7] Karimi, G., Banitalebi, R., & Sedaghat, S. B. (2013). Simulation of SiGe:C HBTs using neural network and adaptive neuro-fuzzy inference system for RF applications. *International Journal of Electronics*, 100(7), 959–975. doi:10.1080/00207217.2012.727353.
- [8] Zolfaghari, A., & Razavi, B. (2003). A low-power 2.4-GHz transmitter/receiver CMOS IC. *IEEE Journal of Solid-State Circuits*, 38(2), 176-183.
- [9] Abbasnezhad, F., Seifi, Z. (2025). High-Efficiency L-Band GaN Power Amplifier Employing Second and Third Harmonic Impedance Optimization, *Contrib. Sci. & Tech Eng*, 2(4). doi:10.22080/cste.2025.29172.1044.
- [10] Karimi, G., Sedaghat, S. B., & Banitalebi, R. (2013). Designing and modeling of ultra low voltage and ultra low power LNA using ANN and ANFIS for Bluetooth applications. *Neurocomputing*, 120, 504–508. doi:10.1016/j.neucom.2013.04.021.
- [11] Karimi, G. R., & Sedaghat, S. B. (2012). Ultra low voltage, ultra low power low noise amplifier for 2 GHz applications. *AEU - International Journal of Electronics and Communications*, 66(1), 18–22. doi:10.1016/j.aeue.2011.04.008.
- [12] Sedaghat, S. B., Safari, F., Karimi, G. R., Alizadeh, S. M., & Banitalebi, R. (2012). 0.3 V, 0.5 mW Low Noise Amplifier for 5.1 GHz Applications. *International Journal on Communications Antenna and Propagation (I.Re.C.A.P.)*, 2(3), 166-170.
- [13] Salighe, E., & Mojarad, M. (2023). A linearity enhancement technique for low-noise transconductance amplifiers in SAW-less receivers. *AEU - International Journal of Electronics and Communications*, 160, 154499. doi:10.1016/j.aeue.2022.154499.
- [14] Sharma, K., Singh, S., & Sachdeva, A. (2024). A low-power low-noise amplifier with high CMRR for wearable healthcare applications. *AEU - International Journal of Electronics and Communications*, 173. doi:10.1016/j.aeue.2023.154994.
- [15] Bisht, R., Akhtar, M. J., & Qureshi, S. (2020). Design of reconfigurable multi-band low-noise amplifiers for 802.11ah/b/g and DCS-1800 applications. *AEU - International Journal of Electronics and Communications*, 120, 153201. doi:10.1016/j.aeue.2020.153201.
- [16] Aneja, A., Li, X. J., & Chong, P. H. J. (2021). Design and analysis of a 1.1 and 2.4 GHz concurrent dual-band low noise amplifier for multiband radios. *AEU - International Journal of Electronics and Communications*, 134. doi:10.1016/j.aeue.2021.153654.
- [17] Javanbakht, P., & Mojarad, M. (2023). A Low-Noise Amplifier with Bandwidth Extension and Noise Cancellation for 5G Receivers. 2023 5th Iranian International Conference on Microelectronics, IICM 2023, 155–159. doi:10.1109/IICM60532.2023.10443108.
- [18] Snehaltha, J., & Singh, A. (2024). A high linearity wideband common-gate LNA with modified differential inductor. *E-Prime - Advances in Electrical Engineering, Electronics and Energy*, 8, 100528. doi:10.1016/j.prime.2024.100528.
- [19] Karimia, G. R., & Banitalebi, R. (2011). A novel small-signal modeling and simulation technique in SiGe:C HBT for ultra high frequency applications. *IEICE Electronics Express*, 8(5), 299–305. doi:10.1587/elex.8.299.
- [20] Lee, K., Choi, K., Kook, S. H., Cho, D. H., Park, K. W., & Kim, B. (2005). Direct parameter extraction of SiGe HBTs for the VBIC bipolar compact model. *IEEE Transactions on Electron Devices*, 52(3), 375–384. doi:10.1109/TED.2005.843906.
- [21] Yun, S., Cho, J., Jo, S., Hwang, I.-C., Kim, Y., Jeong, S., Lee, J., Lee, S., Kim, K., Yoo, S., Han, S., & Kwon, K. (2023). A 2.4/5 GHz Dual-Band Low-Noise and Highly Linear Receiver With a New Power-Efficient Feedforward OPAMP for WiFi-6 Applications. *IEEE Access*, 11, 137264–137273. doi:10.1109/access.2023.3339573.
- [22] Zaid, M., Kumari, P., Pampori, A., Nazir, M. S., Goyal, U., Mishra, M., & Chauhan, Y. S. (2024). Optimizing Low Noise Amplifiers: A Two-Stage Approach for Improved Noise Figure and Stability. *IEEE Access*, 12, 53475–53484. doi:10.1109/ACCESS.2024.3387108.
- [23] Rahman, M., & Harjani, R. (2018). A 2.4-GHz, Sub-1-V, 2.8-dB NF, 475-Dual-Path Noise and Nonlinearity Cancelling LNA for Ultra-Low-Power Radios. *IEEE Journal of Solid-State Circuits*, 53(5), 1423–1430. doi:10.1109/JSSC.2017.2786736.
- [24] Lee, M., Elbadry, M. M., & Moez, K. (2024). A 300- μ W 2.4-GHz PVT-Insensitive Subthreshold Reference-Based LNA. *IEEE Journal of Solid-State Circuits*, 59(9), 2747–2760. doi:10.1109/JSSC.2024.3375154.
- [25] Shirmohammadi, B., & Yavari, M. (2022). A Linear Wideband CMOS Balun-LNA with Balanced Loads. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 69(3), 754–758. doi:10.1109/TCSII.2021.3105895.
- [26] Snehitha Reddy, T., & Nath, V. (2025). A 180 nm CMOS dual-mode LNA with current reuse and double-resonance load for 2.4 GHz and 3.1–10.6 GHz wireless communication. *Scientific Reports*, 15(1). doi:10.1038/s41598-025-93530-3.
- [27] Zhang, M., Cheng, Z., Gong, T., Zheng, B., Zhiwei Zhang, Z., & Xuan, X. (2025). Design of a Dual-Band Low-Noise Amplifier with a Novel Matching Structure. *Micromachines*, 16, 938. doi:10.3390/mi16080938.