RESEARCH PAPER
Contrib. Sci. & Tech Eng, 2026, 3(2)
Homepage: https://cste.journals.umz.ac.ir/
DOI: 10.22080/cste.2026.30337.1089

A Transformerless Dual-Stacked Boost High Step-Up DC–DC Converter with Voltage Multiplier Cells for Photovoltaic Applications

Manoochehr Gorji [1], Amirhossein Riyahi [1], Mohsen Hamzeh [1]*

[1] *School of Electrical and Computer Engineering, University of Tehran, Tehran, Iran.*

Article Info
Received 30 October 2025
Accepted 25 January 2026
Available online 31 May 2026

Keywords:
DC-DC Converter;
High Gain;
Photovoltaic;
Stacked Boost;
Transformerless.

Abstract:

This paper presents a novel transformerless dual-stacked boost DC-DC converter integrated with voltage multiplier cells (VMCs), specifically designed to address the ultra-high voltage gain requirement in PV applications. The proposed structure achieves an exceptionally high voltage conversion ratio using a moderate duty cycle while ensuring low voltage stress on the main power switches. The converter's operation and performance were validated through comprehensive simulation studies conducted at a switching frequency (f_s) of 50 kHz. Open-loop simulations confirmed the static gain capability, demonstrating a voltage gain of 16 times by boosting a 20 V input to an output of approximately 320 V at a duty cycle of 50%. Furthermore, the converter's dynamic performance was rigorously assessed in a closed-loop environment by integrating it with a PV array and an MPPT controller. This setup confirmed the ability to regulate the DC bus voltage at 380 V while effectively tracking the Maximum Power Point (MPP). The results confirm that the proposed converter provides a structurally simple and highly effective solution for high-gain power conversion in renewable energy systems.

***Corresponding Author:** mohsenhamzeh@ut.ac.ir

Supplementary information: Supplementary information for this article is available at https://cste.journals.umz.ac.ir/

Please cite this paper as: Gorji, M. , Riyahi, A. Hossein, & Hamzeh, M. (2026). A Transformerless Dual-Stacked Boost High Step-Up DC–DC Converter with Voltage Multiplier Cells for Photovoltaic Applications. Contributions of Science and Technology for Engineering, 3(2), 71-84. doi:10.22080/cste.2026.30337.1089.

1. Introduction

The rapid growth of distributed DC applications, such as photovoltaic systems, fuel cells, and energy storage units, has created a rising demand for non-isolated DC–DC converters. These converters must offer high voltage gain, high efficiency, and desirable power density [1, 2]. Transformerless converters are regarded as cost-effective and attractive due to their structural simplicity, compact size, and reliance on standard components. However, achieving an ultra-high voltage conversion ratio without excessively extending the duty cycle is challenging. Simultaneously, maintaining high efficiency remains a primary challenge in this field [3-5].

Conventional approaches to improve voltage gain can be categorized into two groups. The first relies on coupled and multi-winding inductors. These can achieve very high gain but require a bulky and complex magnetic design. The second group uses transformerless topologies that employ voltage-lift cells, switched-capacitor or switched-inductor networks, or stacked boost stages to enhance modular gain [6-8]. Multiplier-cell-based methods help reduce voltage stress on components. However, the charging and discharging losses of capacitors, along with inrush currents during switching transitions, may reduce overall efficiency. Stacking multiple boost stages can exponentially increase theoretical gain. Yet, parasitic effects and conduction losses often reduce the practical conversion ratio [9-12].

Recent studies have demonstrated that combining stacked boost structures with voltage-lift cells is an effective approach for achieving high gain at moderate duty cycles without transformers [13-15]. Nevertheless, several important research gaps remain in this area. These include the lack of comprehensive models that account for practical parasitic components [1, 10], the need for detailed investigation of voltage distribution and loss management in multi-stage architectures [8, 12], and the absence of robust engineering solutions to mitigate inrush currents and electromagnetic interference (EMI) in capacitor-based cells [6, 13]. Recent efforts have sought to address these challenges by introducing new topologies, enhancing multiplier networks, and recovering leakage energy, thereby bringing the practical conversion gain closer to its theoretical value while improving power density and efficiency [15, 16]. This research trend is expected to continue, leading to the development of simpler, more cost-effective, and highly efficient converter structures in the years to come.

*ISSN **3060-6578***

A transformerless dual-stacked boost converter integrated with voltage multiplier cells (VMCs) is proposed, in which the strategic stacking of two boost stages—combined with capacitive voltage-multiplying mechanisms—provides an ultra-high step-up gain at moderate duty cycles while maintaining significantly reduced voltage stress on the active switches compared with conventional stacked or quadratic high-gain converters. The dual-stage stacked arrangement not only enhances the conversion ratio but also ensures continuous input and output currents, thereby minimizing current ripple and enabling direct interfacing with photovoltaic sources and other sensitive DC loads. Furthermore, the topology preserves a common ground between input and output, facilitating seamless integration into PV and energy-storage-based architectures. To enable accurate prediction of practical performance, a comprehensive non-ideal, loss-aware analytical model is developed that incorporates the inductor DC resistance, the MOSFET on-state resistance, and the diode forward-voltage drops. Sensitivity analyses are conducted to quantify the influence of component quality and output power on voltage gain and efficiency. System-level validation is also provided by coupling the converter with a realistic PV module model and an MPPT+PI control loop; the closed-loop time-domain simulations confirm stable maximum power point tracking and robust DC-bus regulation.

Overall, the innovative dual-stacked boost configuration together with integrated VMCs, supported by a detailed non-ideal model and control-level validation, delivers high voltage gain, continuous current profiles, reduced semiconductor stress, and common-ground capability—clearly distinguishing the proposed topology from existing high-gain architectures.

The remainder of the paper is organized as follows. Section 2 describes the proposed converter topology and its operating modes. Section 3 compares the proposed converter with recent studies. Section 4 presents the simulation results, including detailed PLECS power-stage waveforms and system-level MATLAB/Simulink studies of the photovoltaic module with MPPT and voltage regulation. Section 5 concludes the paper by summarizing the main findings and contributions.

2. Proposed Topology

The proposed converter features a hybrid architecture specifically designed to achieve a high voltage gain. The fundamental structure is based on the cascading and stacking of two classical boost converters. In this configuration, each boost converter operates as an independent stage, while its outputs are connected in series. This series connection allows the total output voltage to be the sum of the voltages generated by each stage, constituting the first level of voltage amplification in the topology. To further enhance the voltage gain, voltage multiplier cells (VMCs) are incorporated into the baseline structure. These cells, consisting of simple diode–capacitor combinations, operate on the charge-pump principle. During switching cycles, they store energy in their inductors and capacitors and subsequently add it to the output voltage. In effect, these cells apply a secondary voltage boosting mechanism on top of the cascaded structure. As a result, the final output voltage is achieved through the synergistic contribution of both mechanisms, enabling the converter to realize a substantial voltage gain without requiring an excessively high duty cycle. Figure 1 illustrates the design process and the development of the proposed topology.

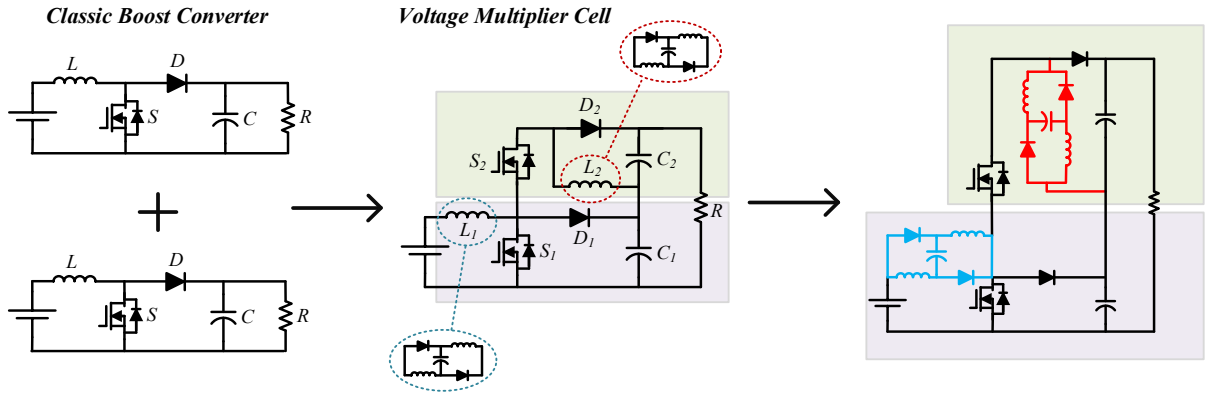

Figure 1. Design process and development of the proposed converter

The topology of the proposed converter is shown in Figure 2. The circuit comprises two switches, four inductors, four capacitors, and six diodes.

The converter operates in two distinct modes, with the corresponding equivalent circuits depicted in Figure 3. In the first mode, both switches S_1 and S_2 are turned ON. This mode represents the energy storage phase of the inductors. In this condition, the input source current flows through switch S_1 and diode D_2, storing energy in inductors L_1 and L_2 as well as capacitor C_1. Simultaneously, switch S_2enables energy storage in inductors L_3 and L_4 and capacitor C_3, charging them accordingly. Throughout this interval, the load R is supplied by the energy previously stored in the main output capacitors C_2 and C_4. In the second mode, both switches S_1 and S_2 are turned OFF, and the circuit transitions into the energy transfer phase. At this stage, the inductors release their stored energy. Specifically, the magnetic energy in L_1 and L_2, combined with the energy from C_1, is transferred through diode D_3 to capacitor C_2, thereby charging it. Similarly, the energy stored in L_3 and L_4, together with C_3, is transferred via diode D_6 to capacitor C_4 in the final output stage. This continuous cycle of energy storage in the inductors and capacitors during the ON-state of the switches, followed by energy transfer to the output

capacitors during the OFF-state, results in a multi-stage voltage-boosting effect. Consequently, the proposed converter achieves a significantly high voltage gain.

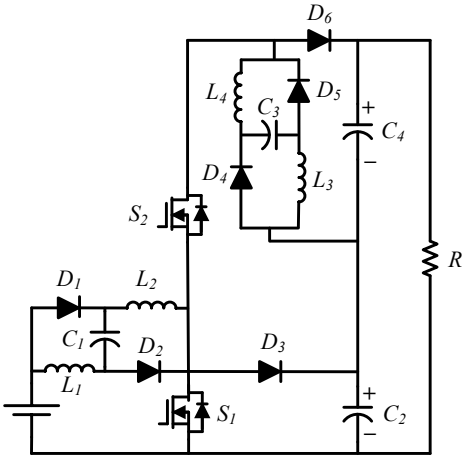

Figure 2. The proposed topology

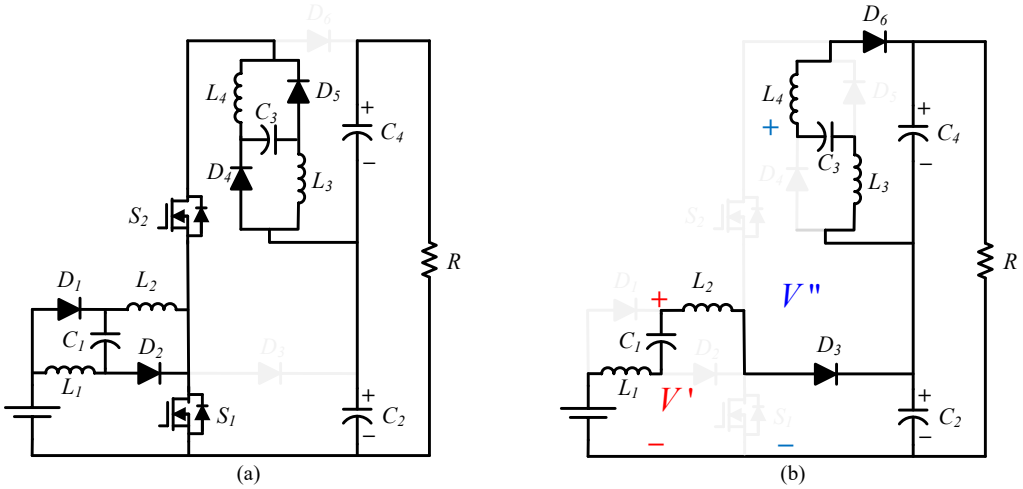

Figure 3. The equivalent circuit of the: (a) first mode, (b) the second mode

Based on the equivalent circuits corresponding to the first and second operating modes, the voltage equations of the inductors and the current equations of the capacitors can be expressed as in Equation 1.

$$\begin{cases} V_{L_1} = L_1 \dfrac{di_{L_1}}{dt} = D(V_{in}) + (1-D)(V_{in} - V' + V_{C_1}) \\ V_{L_2} = L_2 \dfrac{di_{L_2}}{dt} = D(V_{C_1}) + (1-D)(V' - V_{C_2}) \\ V_{L_3} = L_3 \dfrac{di_{L_3}}{dt} = D(V_{C_2}) + (1-D)(V_{C_2} - V'' - V_{C_3}) \\ V_{L_4} = L_4 \dfrac{di_{L_4}}{dt} = D(V_{C_2}) + (1-D)(V'' - V_{C_4} - V_{C_2}) \end{cases}, \quad \begin{cases} i_{C_1} = C_1 \dfrac{dV_{C_1}}{dt} = D(i_1) + (1-D)(-i_{L_1}) \\ i_{C_2} = C_2 \dfrac{dV_{C_2}}{dt} = D(-I_o - i_{L_3} - i_{L_4} + i_3) + (1-D)(i_{L_1} - I_o) \\ i_{C_3} = C_3 \dfrac{dV_{C_3}}{dt} = D(i_3) + (1-D)(-i_{L_3}) \\ i_{C_4} = C_4 \dfrac{dV_{C_4}}{dt} = D(-I_o) + (1-D)(i_{L_3} - I_o) \end{cases} \tag{1}$$

where $V_{L_{1-4}}$ and $i_{L_{1-4}}$ denote the voltages and currents of inductors L_1, L_2, L_3, and L_4, while $V_{C_{1-4}}$ and $i_{C_{1-4}}$ represent the voltages and currents of capacitors C_1, C_2, C_3, and C_4, V_{in} is the input voltage, I_o is the output current, i_3 is the inrush current of C_3, and D is the duty cycle of the converter. By applying the volt-second balance principle to the inductor voltage equations and the charge balance principle to the capacitor current equations, the average values of the capacitor voltages and inductor currents, as well as the ideal voltage gain of the converter, can be derived, as shown in Equation 2.

Once the average capacitor voltages and inductor currents are obtained, the voltage and current stresses imposed on the semiconductor devices can be determined. These stresses are expressed in Equation 3.

By normalizing the voltage stresses to the output voltage and the current stresses to the input current, the results shown in Figure 4 are obtained. Since, in high-gain converters, the maximum voltage typically appears at the output and the maximum current at the input, selecting these values as the basis for normalization is both logical and well-justified.

$$\begin{cases} V_{C_1}=V_{in}\ ,\ V'=\dfrac{2-D}{1-D}V_{in} \\ V_{C_2}=V_{C_3}=\dfrac{2}{(1-D)^2}V_{in}\ ,\ V''=\dfrac{2(2-D)}{(1-D)^2}V_{in} \\ V_{C_4}=\dfrac{2(1+D)}{(1-D)^2}V_{in}\ ,\ V_o=\dfrac{4}{(1-D)^2}V_{in} \end{cases}\quad \begin{cases} i_{L_1}=i_{L_2}=\dfrac{2}{(1-D)^2}I_o \\ i_{L_3}=i_{L_4}=\dfrac{1}{1-D}I_o \\ i_1=\dfrac{2}{D(1-D)}I_o\ ,\ i_3=\dfrac{1}{D}I_o \end{cases} \tag{2}$$

$$\begin{cases} V_{D_1}=V_{D_2}=\dfrac{1}{1-D}V_{in}\ ,\ V_{D_3}=V_{S_1}=\dfrac{2}{1-D}V_{in} \\ V_{S_2}=\dfrac{2(1+D)}{(1-D)^2}V_{in}\ ,\ V_{D_4}=V_{D_5}=\dfrac{1}{(1-D)^2}V_{in} \\ V_{D_6}=\dfrac{4}{(1-D)^2}V_{in} \end{cases}\quad \begin{cases} I_{S_1}=\dfrac{3+2D-D^2}{(1-D)^2}I_o\ ,\quad I_{S_2}=\dfrac{1+D}{1-D}I_o \\ I_{D_1}=I_{D_2}=\dfrac{2}{(1-D)^2}I_o\ ,\ I_{D_3}=\dfrac{2}{1-D}I_o \\ I_{D_4}=I_{D_5}=\dfrac{1}{1-D}I_o\ ,\ I_{D_6}=I_o \end{cases} \tag{3}$$

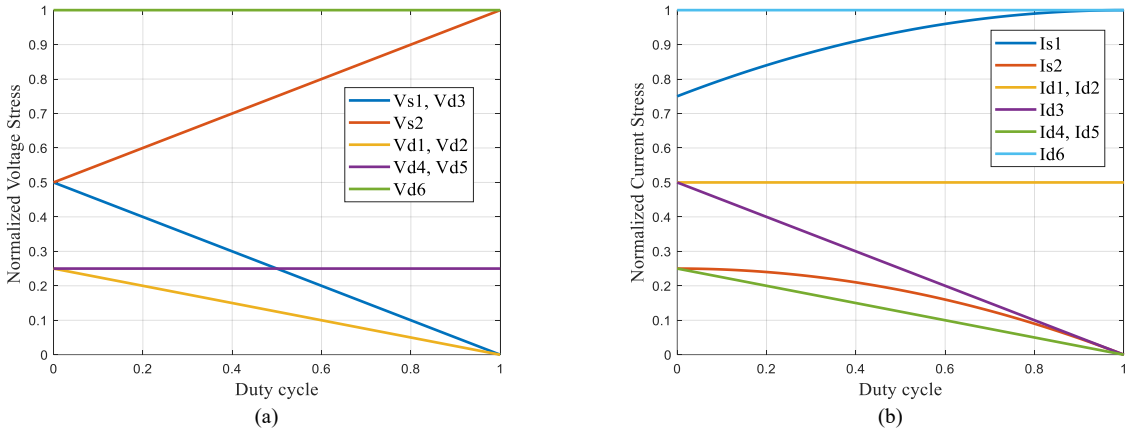

Figure 4. Normalized semiconductor stresses: (a) voltage stress and (b) current stress

From the results of the stress analysis, it can be concluded that the voltage applied across all semiconductor devices except the diode D_6, which experiences a stress equal to unity—remains lower than the converter output voltage. Similarly, the current stresses on all semiconductor devices are consistently lower than the input current. This feature ensures that the proposed converter achieves the desired voltage gain while subjecting its semiconductor components to relatively lower voltage and current stresses. In other words, the currents through the devices remain below the input current, and the voltages applied across them remain below the output voltage. Finally, using the inductor voltage and capacitor current equations, the inductor current ripple and the capacitor voltage ripple can be calculated as given in Equation 4.

Based on the derived expressions for the inductor current ripple, the minimum inductance required to ensure continuous conduction mode (CCM), as well as the output current in terms of the ripple of the last-stage inductor current, are presented in Equation 5.

$$\begin{cases} \Delta i_{L_1}=\dfrac{DV_{in}}{L_1f_s}\ ,\ \Delta i_{L_2}=\dfrac{DV_{in}}{L_2f_s} \\ \Delta i_{L_3}=\dfrac{2DV_{in}}{(1-D)L_3f_s}\ ,\ \Delta i_{L_4}=\dfrac{2DV_{in}}{(1-D)L_4f_s} \end{cases}\quad \begin{cases} \Delta V_{C_1}=\dfrac{2I_o}{(1-D)C_1f_s}\ ,\ \Delta V_{C_2}=\dfrac{\left(1+2D-D^2\right)I_o}{(1-D)C_2f_s} \\ \Delta V_{C_3}=\dfrac{I_o}{C_3f_s}\ ,\ \Delta V_{C_4}=\dfrac{DI_o}{C_4f_s} \end{cases} \tag{4}$$

$$\begin{cases} L_1,L_2\geq\dfrac{D(1-D)^4R}{16f_S} \\ L_3,L_4\geq\dfrac{D(1-D)^2R}{8f_S} \end{cases}\quad \begin{cases} I_o=\dfrac{V_{in}}{2L_3f_s}D \\ I_o=\dfrac{V_o}{8L_3f_s}D(1-D)^2 \end{cases} \tag{5}$$

From the relationship between the average inductor current and the ripple of the last-stage inductor, the operating regions of the converter in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) can be determined as a function of the output current and duty cycle, as illustrated in Figure 5.

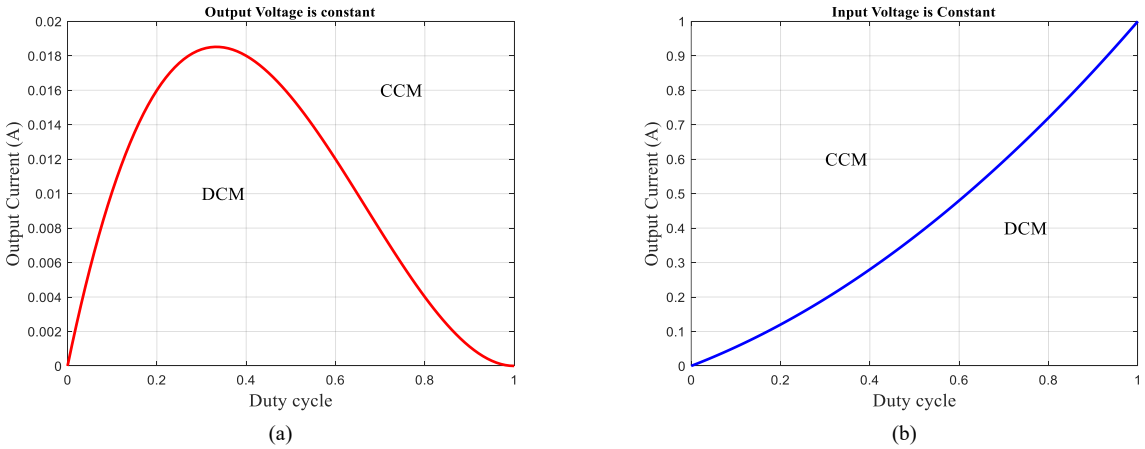

Figure 5. Continuous and discontinuous conduction mode regions based on output current and duty cycle for: (a) constant output voltage and (b) constant input voltage

In this figure, the points below the boundary curves correspond to the DCM region, the points above represent the CCM region, and the points lying exactly on the curves denote the boundary condition between the two modes.

Considering the parasitic elements of the circuit components, including inductor resistance, the internal resistances of the switches and diodes, the non-ideal voltage gain of the proposed converter can be derived as in Equation 6. A comparison between the ideal and non-ideal voltage gains is presented in Figure 6. As shown, for duty cycle values below 50%, the two curves closely match and yield nearly identical values. This agreement indicates that within this duty-cycle range, the influence of non-idealities, such as voltage drops and series resistances, is negligible. However, as the duty cycle increases beyond 50%, the discrepancy between the ideal and non-ideal gain gradually becomes more pronounced. This divergence originates from the effects of non-ideal factors such as internal resistances, power losses, and voltage drops across the semiconductor devices, which become more significant as the operating point approaches maximum input power. This analysis highlights the necessity of accounting for these deviations in the design of high-gain converters, particularly under high-duty-cycle conditions.

$$\frac{V_o}{V_{in}} = \frac{4}{(1-D)^2}\left\{1 - \frac{r_L}{R}\left(\frac{1}{(1-D)^3}\right) - \frac{r_S}{R}\left(\frac{4+2D-2D^2}{(1-D)^4}\right) - \frac{r_D}{R}\left(\frac{2-D}{(1-D)^3}\right)\right. \tag{6}$$

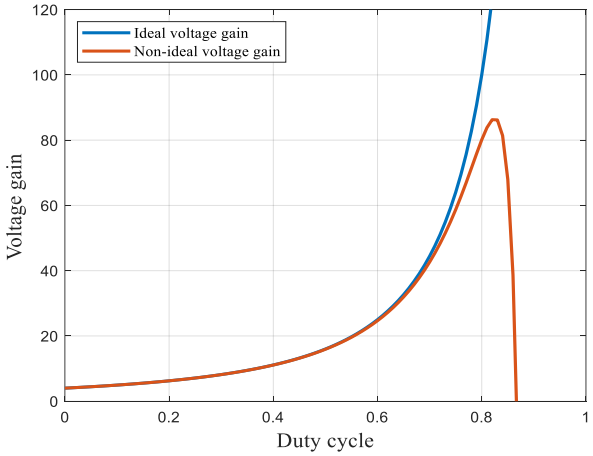

Figure 6. Ideal and non-ideal voltage gains comparison

Moreover, the derived relation enables evaluation of the converter gain performance with respect to variations in output power level, diode characteristics, inductor parameters, and switch properties. Figure 7 illustrates the non-ideal gain response of the converter under these parameter variations. According to the figure, changes in the output power level exhibit the most significant influence on the gain behavior, far exceeding the impact of other factors.

In addition, when considering the parasitic elements of the circuit components, the input and output powers of the converter are no longer equal. By incorporating the conduction losses of the inductors, switches, and diodes, the efficiency of the proposed converter can be modeled as given in Equation 7. Based on the simulation parameters and estimated practical component values, the converter losses are evaluated under operating conditions of 100 W output power, 50 kHz switching frequency, 50% duty cycle,

and 20 V input voltage. In this analysis, the inductor series resistance ($R_L = 0.1$), the MOSFET on-state resistance ($R_{ON} = 0.05$), and the diode forward-voltage drop ($V_{DF} = 0.7$) are taken into account. In addition, the switching losses of the semiconductor devices are approximated at 0.5–1 W. Based on these assumptions, the total converter losses are estimated at 6–7 W.

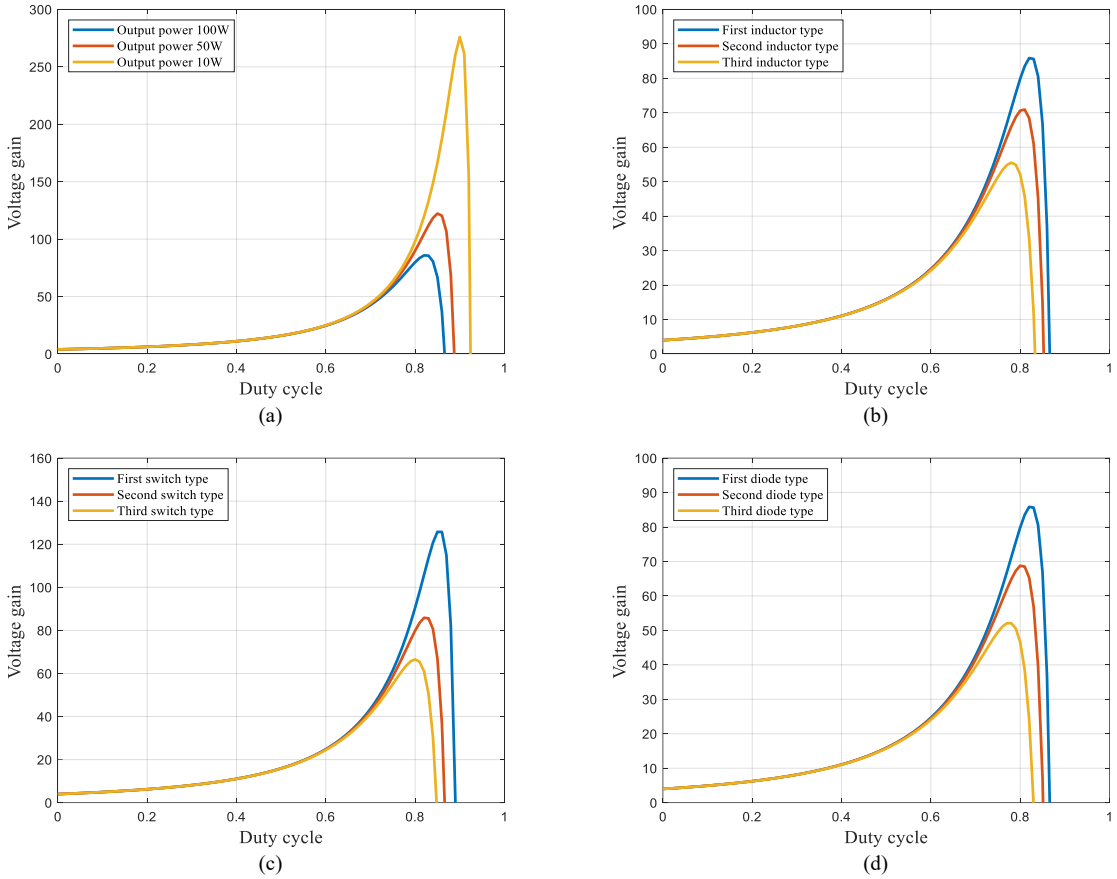

Figure 7. Sensitivity of the nonideal voltage gain to (a) output power, (b) inductor parameters, (c) switch parameters, and (d) diode parameters

$$\begin{cases} P_L = \dfrac{r_L}{R} P_o \dfrac{2\left(5-2D+D^2\right)}{\left(1-D\right)^4} \\ P_{SC} = \dfrac{r_S}{R} P_o \dfrac{10+12D-4D^2-4D^3+2D^4}{2D\left(1-D\right)^4} \\ P_D = V_{DF} I_o \dfrac{9-12D+D^2}{\left(1-D\right)^2} \end{cases} \Rightarrow \boxed{\eta = \frac{P_o}{P_o + P_L + P_{SC} + P_D + P_{SW}}} \tag{7}$$

Table 1 presents the performance of the proposed topology under different operating conditions and output power levels. In this table, the analyses and calculations are performed using the non-ideal, loss-aware model, and the estimated contributions of the main component losses and the overall converter efficiency are reported for each operating case. The assumptions and parameters used in these calculations are specified in the preceding subsection. This approach enables a more objective and fair comparison among different converter topologies and contributes to a clearer assessment of the practical advantages and limitations of the proposed design.

Based on this relation, variations in converter efficiency can be analyzed with respect to changes in output power level and the quality of circuit components, such as inductors, switches, and diodes. Figure 8 clearly illustrates how different factors affect the converter's efficiency.

Table 1. Estimated performance of the proposed converter at different output-power levels2

Output Power	P_L	P_{SC}	P_D	P_{Loss}	Efficiency
50 W	0.34 W	0.3 W	1.4 W	2.04 W	95.8%
100 W	1.32 W	1.14 W	2.73 W	5.19 W	94/%
150 W	2.98 W	2.59 W	3.64 W	9.21 W	92.1%

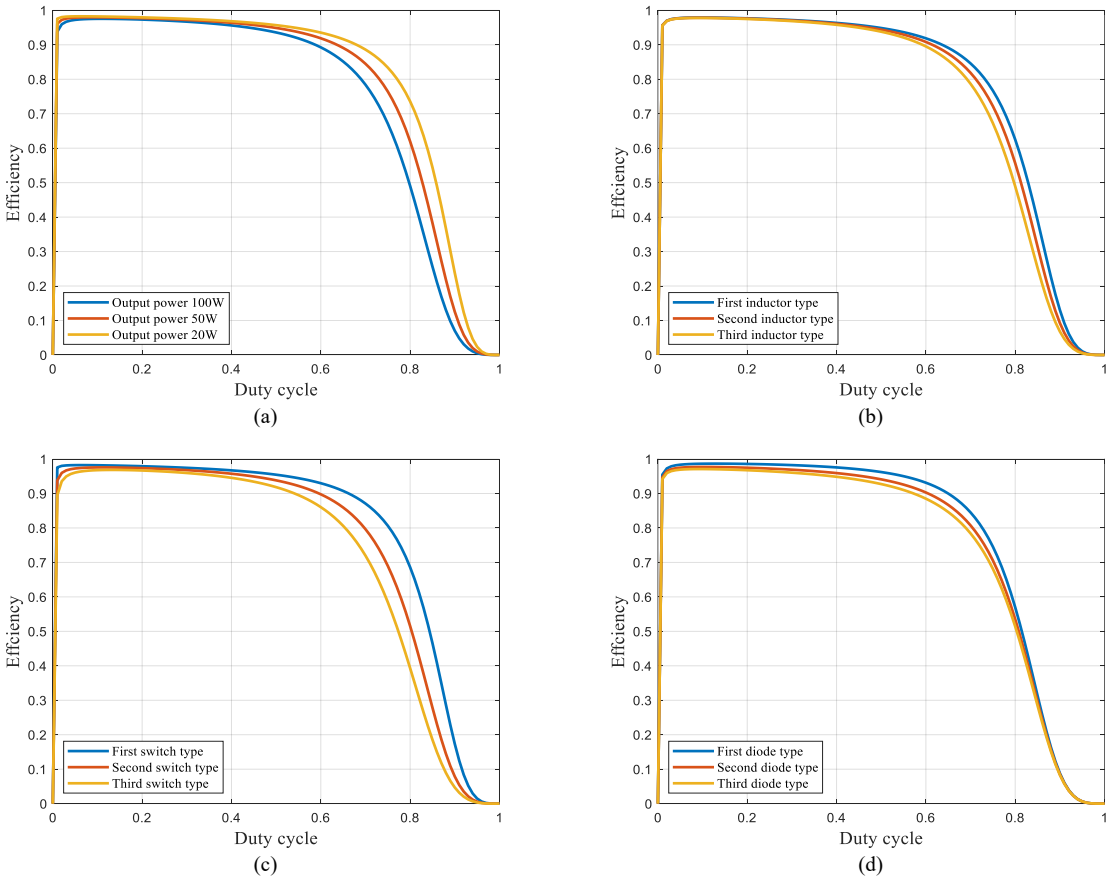

Figure 8. Sensitivity of the estimated efficiency to (a) output power, (b) inductor parameters, (c) switch parameters, and (d) diode parameters

As shown in Figure 8, the output power level exerts the most significant impact on converter efficiency. With increasing output power, the losses associated with internal resistances of passive elements and the voltage drops across diodes and switches increase considerably, resulting in a noticeable reduction in system efficiency. In addition to the power level, the quality of the components used also plays a crucial role in determining efficiency. Enhancing inductor quality by reducing their equivalent series resistance and using diodes and switches with lower voltage drops can substantially improve efficiency at high power levels. Conversely, employing low-quality components, particularly in high-power conditions, leads to a considerable reduction in efficiency. This analysis demonstrates that, to achieve optimal efficiency, not only the selection of an appropriate duty cycle but also the use of high-quality components and careful design are essential. Moreover, the effect of output-power variation on efficiency must be considered a key factor in the design of high-gain DC–DC converter systems.

3. Comparison of the Proposed Converter with Recent Researches

In the previous section, the proposed converter was thoroughly analyzed and evaluated. This section aims to assess and compare its overall performance with several converters reported in recent studies. Figure 9 compares the voltage gain of the proposed topology with that of converters introduced in recent works. As observed, the proposed converter consistently achieves a higher voltage gain over the entire duty-cycle range. This result highlights the superiority of the proposed converter in terms of voltage gain, demonstrating its advantage over other topologies on this performance index.

Table 2 provides a comprehensive comparison of different converters based on several criteria, including voltage gain at a duty cycle of 50%, switch voltage stress, design complexity, and efficiency. For each converter, a score is assigned based on its performance on each criterion. The final evaluation index is then obtained by summing these scores, offering a single quantitative metric for assessing the overall performance of the converters under study. This scoring methodology ensures a fair and balanced comparison by assigning greater weight to more significant parameters. Specifically, the weighting factors for voltage gain, switch voltage stress, design complexity, and efficiency were selected as 35%, 25%, 20%, and 20%, respectively. This approach enables a holistic comparison of different topologies, where the final score serves as a reliable benchmark for evaluating both performance and practicality. The results clearly indicate that the proposed converter achieves the highest overall score, thereby validating its effectiveness as a high-gain, efficient, and practical solution compared to recent alternatives.

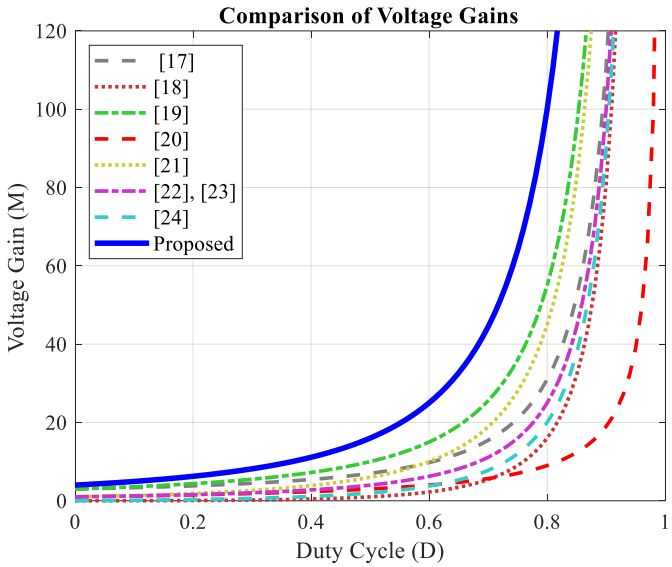

Figure 9. Voltage gain comparison between the proposed topology and the converters presented in recent studies

Table 2. Quantitative comparison of the proposed converter with other converters

Converter	L	S	D	C	Gain	Gain Point of 35	Voltage Stress of Switches	Stress Point of 25	Design Coefficient	Design Point of 20	Efficiency Point of 20	Final Point
Lee et al. [17]	2	2	3	3	7	15	0.85	16	2.3	17	16	64
Rosas-Caro et al. [18]	2	2	2	2	1	2	4	4	2	19	20	45
Mizani et al. [19]	3	2	4	5	10	22	0.6	23	3.1	12	11	68
Rahimi et al. [20]	2	2	2	2	3	7	1.32	11	2	19	20	57
Zhang et al. [21]	2	2	5	5	6	13	0.56	25	2.9	13	11	62
Valdez-Resendiz et al. [22]	2	1	3	2	4	9	1	14	1.9	20	20	63
Gupta et al. [23]	2	2	2	2	4	9	1	14	2	19	20	62
Totonchi et al. [24]	3	2	3	3	2	4	1	14	2.7	14	15	47
Proposed	4	2	6	4	16	35	1	14	3.8	10	10	69

In the first step, to calculate the voltage gain score, the gains of all converters at a 50% duty cycle were evaluated. The converter achieving the highest voltage gain among all candidates was assigned the full score of 35. In contrast, the scores of the remaining converters were determined linearly based on the ratio of their gain to the maximum gain. In the first step, to calculate the voltage gain score, the gains of all converters at a 50% duty cycle were evaluated. The converter achieving the highest voltage gain (G_{Max}) among all candidates was assigned the full score of 35, while the scores of the remaining converters were determined linearly based on the ratio of their gain to the maximum gain.

$$S_{Gain} = \left(\frac{G_i}{G_{Max}}\right) \times 35 \tag{8}$$

For the voltage stress score, the weighted average of the normalized voltage stresses of the switches and the diodes experiencing the highest stress in each converter was calculated. In this evaluation, the weight assigned to switch stresses was twice that of diode stresses, reflecting the greater significance of semiconductor switches in converter performance. For example, if a converter contains two switches with voltage stresses of 0.5 and one diode with a maximum stress of 1, the weighted average stress would be calculated as 0.6. After computing this index for all converters, the topology with the lowest stress (V_{Stress_Min}) received the full score of 35, and the other converters were scored linearly with respect to this best case.

$$S_{Stress} = \left(\frac{V_{Stress\_Min}}{V_{Stress\_i}}\right) \times 25 \tag{9}$$

With regard to the design complexity factor, the adopted metric was the weighted average number of components employed in each converter. The assigned weights for the components were as follows: inductors = 4, switches = 3, diodes = 2, and capacitors = 1. These weights were selected to reflect the greater impact of critical components on overall design complexity. Once this index was calculated for all converters, the converter with the simplest structure (C_{Design_Min}) was awarded the full score of 20, while the others were scored linearly in proportion to this benchmark.

$$S_{Design} = \left(\frac{C_{Design\_Min}}{C_{Design\_i}}\right) \times 20 \tag{10}$$

For the efficiency score, theoretical analyses were repeated for all converters, similar to the proposed topology, by incorporating the effects of parasitic elements (inductors, switches, and diodes). In this evaluation, identical parasitic values, output load, and duty cycle were assumed across all converters to ensure a fair comparison. As with the other parameters, the converter with the highest efficiency (η_{Max}) received the full score of 20, while the remaining converters were assigned linearly scaled scores.

$$S_{Efficiency} = \left(\frac{\eta_i}{\eta_{Max}} \right) \times 20 \tag{11}$$

Finally, by aggregating the scores for each converter across the four parameters, the overall score for each topology was calculated on a scale of 100. This final score provides a weight-dependent basis for comparing the selected topologies. The resulting overall scores are compared in Figure 10.

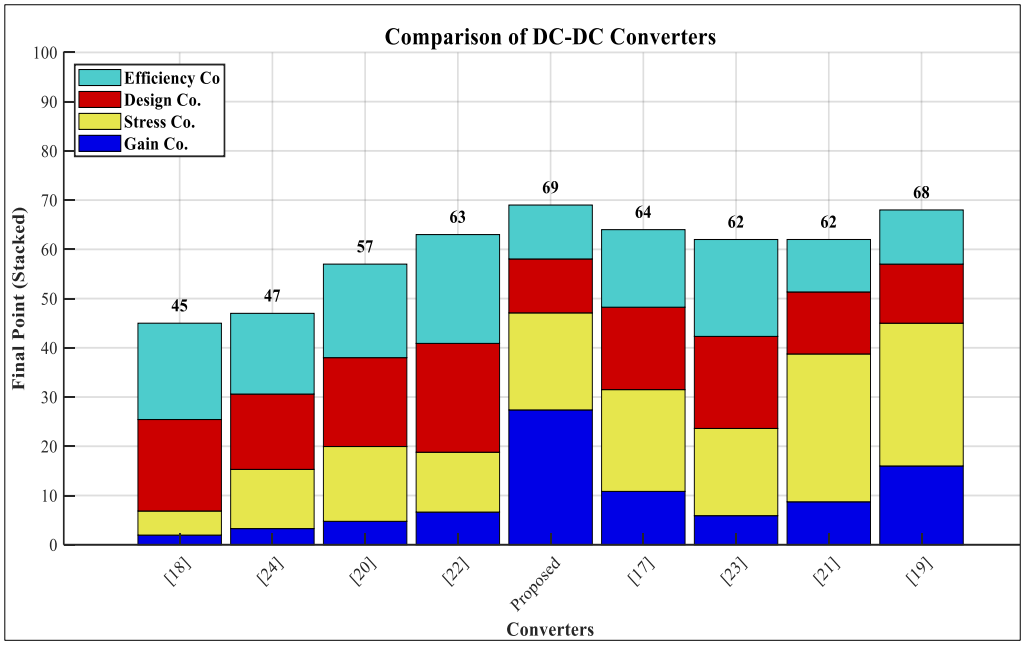

Figure 10. Weighted comparison scores of the proposed and recently reported converters

Based on the comprehensive analysis of the results, a wide spectrum of performance is observed among the investigated DC–DC converters, each reflecting a distinct design philosophy and trade-off among the key parameters of such topologies. At the top of the ranking, the "proposed" converter achieves a score of 69 out of 100, securing the first position. The success of this converter is primarily attributed to its remarkably high voltage gain, while it still maintains acceptable levels of voltage stress and design complexity. This combination renders the proposed topology a highly suitable candidate for applications requiring significant voltage step-up capability.

In high step-up DC–DC converters employed in photovoltaic systems, certain performance metrics—such as voltage gain, semiconductor voltage stress, and conversion efficiency—are of greater significance than other design parameters, as they directly affect the ability of the converter to interface with low-voltage PV sources, ensure device reliability, and maximize energy utilization. Nevertheless, it should be emphasized that the relative weighting of evaluation criteria can lead to different comparative outcomes among converter topologies. These weightings are inherently application-dependent and may vary with system requirements, operating conditions, and power levels. Consequently, the prioritization of design parameters should be adapted to the specific application context, and different sets of performance indices may govern the selection and assessment of an appropriate converter topology.

4. Simulation

The proposed converter was simulated in PLECS software to validate the theoretical analysis. For the simulation, a duty cycle of 0.5, a switching frequency of 50 kHz, an output power of 100 W, an input voltage of 20 V, and an output current of 0.25 A were considered. The converter components were designed accordingly. The inductors were selected to ensure a 30% current ripple, while the capacitors were chosen to ensure a 5% voltage ripple. The simulation was performed with a duty cycle of 50%, a switching frequency of 50 kHz, and an input voltage of 20 V. The required PWM signal for switch control was generated using a Pulse Generator block. Based on these parameters, time-domain simulations were conducted to analyze the converter performance. The corresponding input and output voltage waveforms are illustrated in Figure 11.

Consistent with the theoretical analysis, a voltage gain of 16 was expected and clearly verified by the simulation results. Specifically, for an input voltage of 20 V, the converter achieved an output voltage of approximately 320 V, confirming the predicted gain. The inductor current waveforms are illustrated in Figure 12, where the first and second inductor currents are approximately 2.44 A, while the third and fourth inductor currents are around 0.65 A.

Furthermore, Figure 13 depicts the voltage stresses across the semiconductor devices.

In this section, the proposed converter is connected to a photovoltaic module (REC Solar REC220AE-US) to evaluate its performance under practical PV conditions. The converter output is connected to a DC bus with a regulated 380 V voltage, emulating the connection to a downstream inverter stage. The objective of this test is not to control the DC link voltage, but to verify the converter's and its control scheme's ability to operate the PV module at its maximum power point (MPP) at all times.

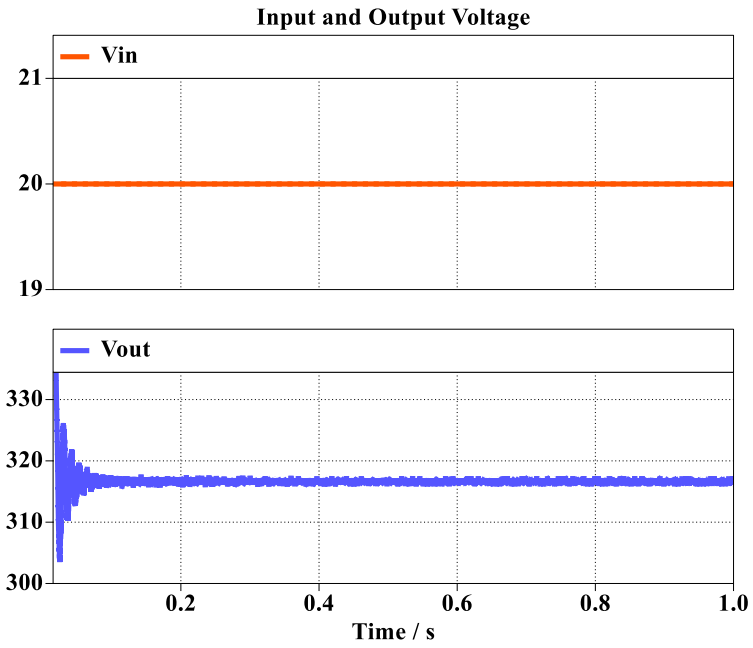

Figure 11. Input- and output-voltage waveforms

The control loop consists of a perturb-and-observe (P&O) maximum power point tracking (MPPT) algorithm that generates a reference voltage, followed by a proportional–integral (PI) controller based on the small-signal model of Vin/d.The PI controller regulates the panel voltage by adjusting the duty cycle of the converter switches. This configuration ensures that the panel voltage converges toward the MPP reference with minimal steady-state error. In the simulation environment, the output side is modeled with an ideal DC voltage source in parallel with a large bus capacitor, ensuring that the MPPT dynamics are isolated from inverter control. As a result, any instantaneous power mismatch between the PV side and the load is temporarily absorbed or supplied by the bus capacitor, allowing clear observation of the MPPT and voltage control loop performance.

To facilitate comparison between simulation results and theoretical expectations, Table 3 summarizes the maximum power point parameters for the selected PV module (REC220AE-US) at three irradiance levels (800 W/m², 900 W/m², and 1000 W/m²), with a constant cell temperature of 25 °C. The parameters include the maximum power point voltage (V_{MPP}), current (I_{MPP}), *and power (PMPP), as* derived from the module datasheet. These values serve as reference benchmarks for evaluating the correctness of the MPPT and control performance in subsequent figures.

Figure 14 illustrates the duty cycle alongside the irradiance profile. After an initial transient, the duty cycle stabilizes at approximately 0.46. This value is entirely consistent with the expected operating point, given the converter's input voltage (the PV module voltage at MPP) and the regulated output voltage of 380 V. Furthermore, the duty cycle exhibits negligible deviation during irradiance transitions, confirming the robustness of the control loop.

Figure 15 presents the PV output power compared with the irradiance profile. At each irradiance level, the extracted power converges to the theoretical maximum power as indicated in the module's datasheet. The stabilization of power at the correct values demonstrates the effectiveness of the MPPT algorithm and the converter's ability to reliably track the MPP under irradiance variations.

Figure 16 shows the PV voltage (V_{PV}) alongside the MPPT-generated reference voltage (V_{ref}). The results confirm that the actual PV voltage follows the reference signal with minimal steady-state error. Across all irradiance scenarios, V_{PV} remains well aligned with V_{ref} , indicating proper operation of the PI controller in enforcing the MPPT command.

Figure 17 depicts the PV current response. The current increases proportionally with irradiance steps and maintains stable operation around the expected maximum power point current (I_{MPP}). This further confirms that the panel's operating point consistently converges to the MPP under dynamic irradiance conditions.

Figure 18 illustrates the converter efficiency profile, obtained by dividing the instantaneous output power by the input power. As observed, the efficiency remains at a desirable level across irradiance variations, demonstrating that the proposed converter not only ensures accurate MPPT tracking but also delivers harvested energy with minimal losses. The stability of the efficiency curve during step

changes confirms that the control strategy does not introduce additional losses or oscillations. Overall, the results validate that the converter achieves a high and consistent efficiency under realistic PV operating conditions.

In summary, the simulation results demonstrate that the proposed converter, together with the MPPT+PI control scheme, ensures stable tracking of the maximum power point. The duty cycle remains at its theoretical value, the panel voltage closely follows the MPPT reference, and both current and power stabilize at the expected values across all irradiance levels. These results confirm both the correctness of the control design and the suitability of the proposed converter for photovoltaic applications

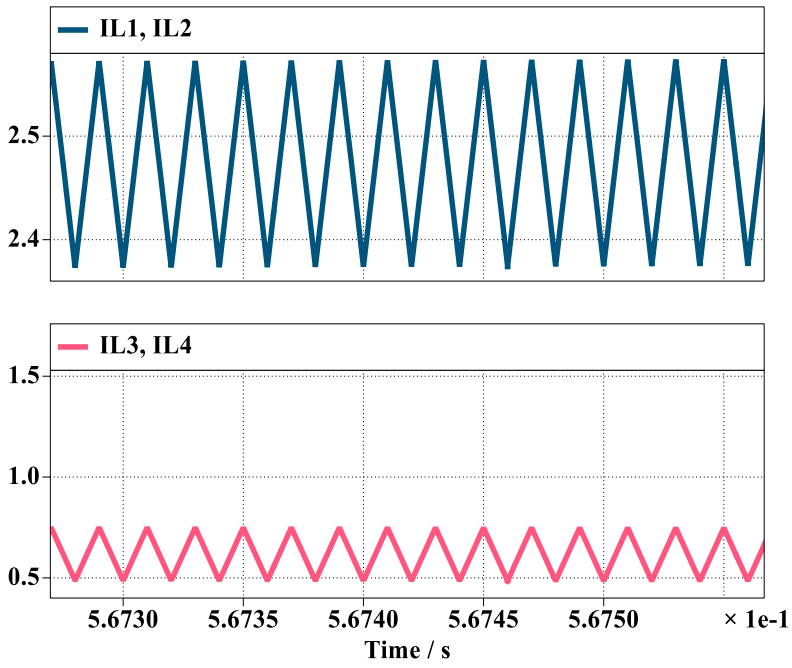

Figure 12. Inductor current waveforms

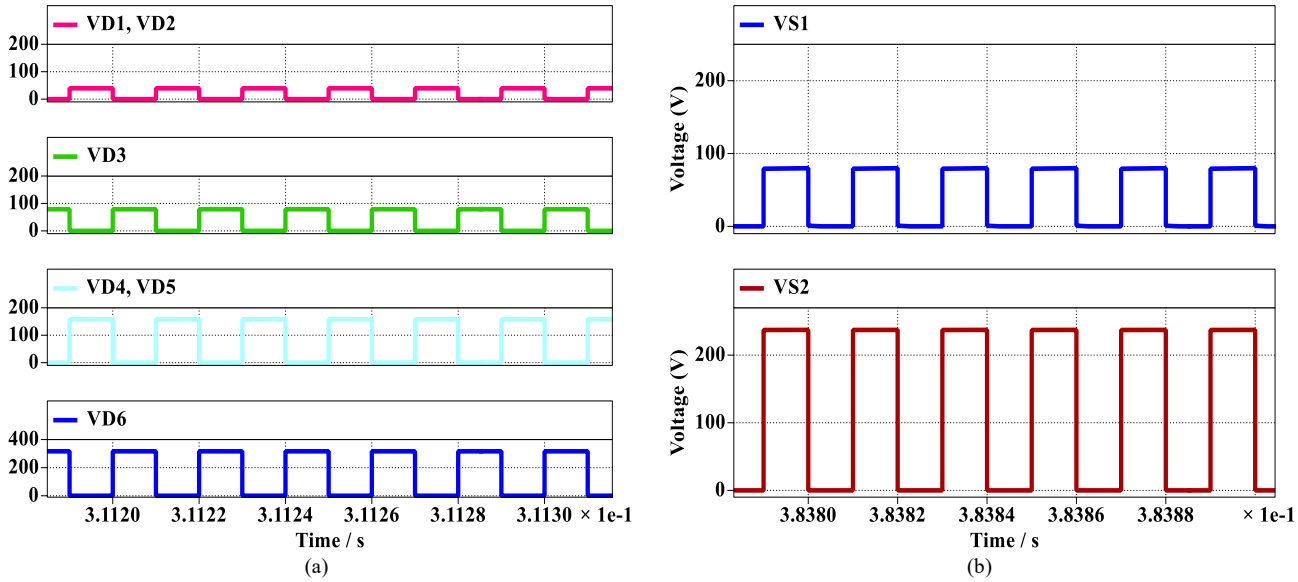

Figure 13. Voltage waveforms of semiconductor devices: (a) switches, (b) diodes

Table 3. Maximum power point parameters for the selected PV module at varying solar irradiance levels at a constant cell temperature of 25 °C

MPP parameter values			*Radiation (W/m²)*
V_{MP} *(V)*	I_{MPP} *(A)*	P_{MPP} *(W)*	
28.70	7.70	220.99	1000
28.7396	6.959	199.998	900
29.0304	6.161	178.863	800

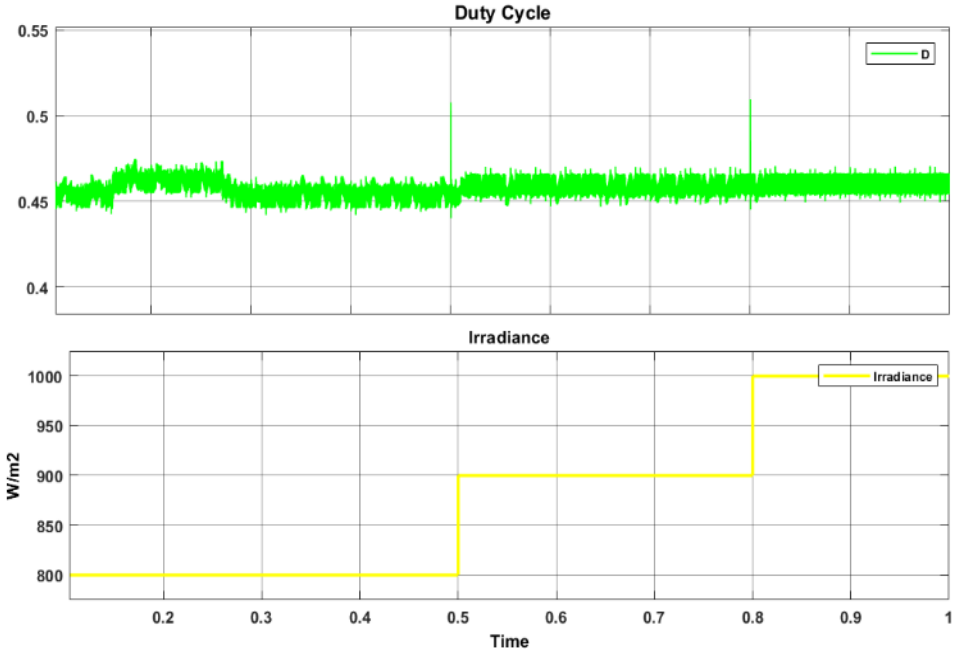

Figure 14. The duty cycle variation alongside the irradiance profile

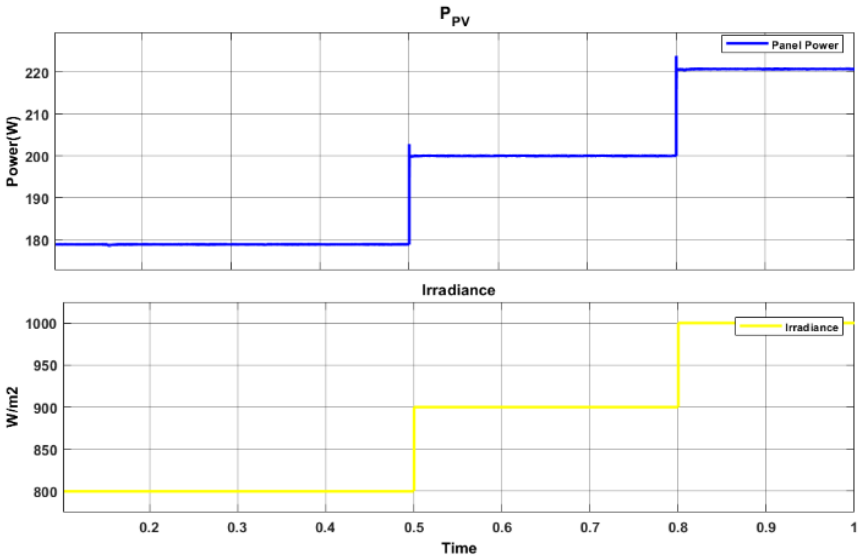

Figure 15. PV output power compared with the irradiance profile

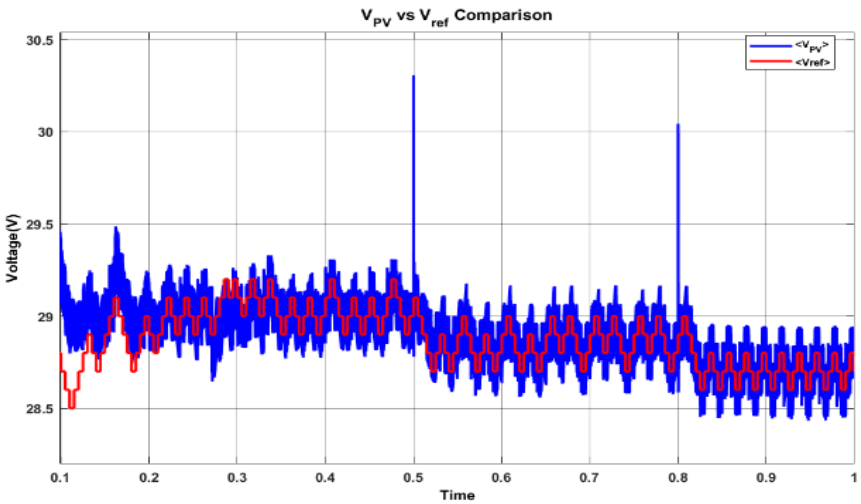

Figure 16. PV voltage alongside the MPPT-generated reference voltage

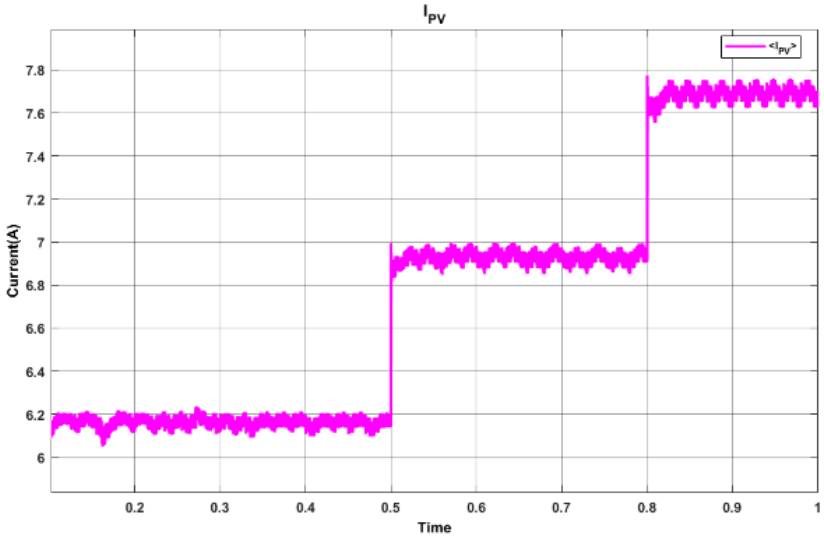

Figure 17. PV current response

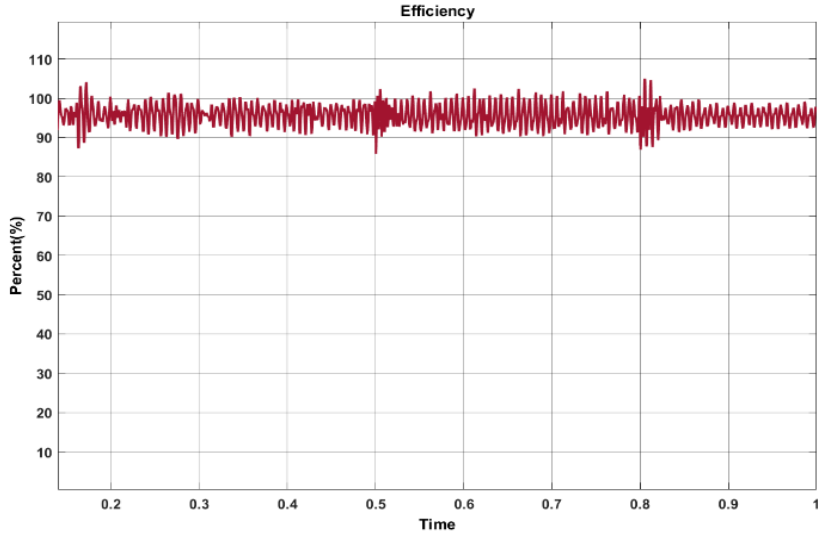

Figure 18. The efficiency profile of the DC–DC converter during operation

5. Conclusion

A dual-stacked boost converter augmented with diode-capacitor multiplier cells is proposed and analyzed, and the results demonstrate that the topology reliably produces large step-up ratios at moderate duty cycles while maintaining continuous input current and a common input-output ground, thereby simplifying photovoltaic integration and reducing electromagnetic interference. A loss-aware analytical model guided component selection to achieve continuous conduction and targeted ripple levels, resulting in inductor current ripple of about 30 percent and output capacitor voltage ripple near 5 percent. Time-domain switching simulations in PLECS with an input voltage of 20 volts, duty cycle of 0.5, switching frequency of 50 kilohertz, and output power of 100 watts produced an output close to 320 volts and device waveforms that closely matched model predictions, showing that most semiconductor voltages remain below the output level. At the same time, a single diode approaches the full output voltage under the chosen normalization. At the system level, a MATLAB Simulink model coupling a REC220AE-US photovoltaic module to a perturb-and-observe maximum power point tracker and a proportional-integral bus-voltage regulator demonstrated robust MPPT convergence for stepped irradiance from 800 to 1000 watts per square meter, with maximum power point voltage around 28.7 to 29.0 volts and current around 6.16 to 7.70 amps, the converter duty cycle stabilizing near 0.46 and conversion efficiency remaining high and stable during transients. Comparative assessment against recent high-gain topologies indicates that the proposed architecture achieves a favorable balance among voltage gain, device stress, and component count, confirming its practical viability for renewable energy interfaces and other applications requiring substantial step-up conversion.

6. References

[1] Hasanpour, S., Siwakoti, Y. P., Mostaan, A., & Blaabjerg, F. (2021). New Semiquadratic High Step-Up DC/DC Converter for Renewable Energy Applications. IEEE Transactions on Power Electronics, 36(1), 433–446. doi:10.1109/TPEL.2020.2999402.

[2] Liang, T. J., Luo, P., & Chen, K. H. (2022). A High Step-Up DC-DC Converter With Three-Winding Coupled Inductor for Sustainable Energy Systems. IEEE Transactions on Industrial Electronics, 69(10), 10249–10258. doi:10.1109/TIE.2021.3123683.

[3] Khan, S., Zaid, M., Siddique, M. D., & Iqbal, A. (2022). Ultra high gain step up DC/DC converter based on switched inductor and improved voltage lift technique for high-voltage applications. IET Power Electronics, 15(10), 932–952. doi:10.1049/pel2.12279.

[4] Marzang, V., Babaei, E., Mehrjerdi, H., Iqbal, A., & Islam, S. (2022). A high step-up DC–DC converter based on ASL and VMC for renewable energy applications. Energy Reports, 8, 12699–12711. doi:10.1016/j.egyr.2022.09.080.

[5] Nadermohammadi, A., Abolhassani, P., Seifi, A., Zarrinehbafan, M., Aghakhanlou, P., Hosseini, S. H., & Sabahi, M. (2024). Cost-effective soft-switching ultra-high step-up DC–DC converter with high power density for DC microgrid application. Scientific Reports, 14(1). doi:10.1038/s41598-024-71436-w.

[6] Fani, R., Farshidi, E., Adib, E., & Kosarian, A. (2020). Analysis, Design, and Implementation of a ZVT High Step-Up DC-DC Converter with Continuous Input Current. IEEE Transactions on Industrial Electronics, 67(12), 10455–10463. doi:10.1109/TIE.2019.2960727.

[7] Karimi, K., Marzang, V., Karimi, M., Hosseini, S. H., & Feyzi, M. R. (2025). High-step-up quadratic DC–DC converter based on switched capacitor and coupled inductor techniques. Scientific Reports, 15(1). doi:10.1038/s41598-025-94214-8.

[8] Duong, V. T., Waheed, Z., & Choi, W. (2025). Non-Isolated Ultra-High Step-Up DC-DC Converter Topology Using Coupled-Inductor-Based Inverting Buck-Boost and Voltage Multipliers. Electronics (Switzerland), 14(13). doi:10.3390/electronics14132519.

[9] Hasanpour, S. (2025). A New Soft-Switched Trans-Inverse Step-Up DC/DC Converter With Zero Input Current Ripple. Energy Science & Engineering, 13(2), 714–727. https://doi.org/10.1002/ese3.2037.

[10] Sharma, P., Hasanpour, S., & Kumar, R. (2024). Enhanced Performance of Cuk and Boost–Based High-Gain Step-Up DC/DC Converter. International Transactions on Electrical Energy Systems, 2024(1). doi:10.1155/2024/3166502.

[11] Hosseini, S. J. A., Hasanpour, S., Shahgholian, G., Moazzami, M., & Baktash, A. (2025). A new ultra-high voltage gain DC/DC converter based on coupled-inductor. Scientific Reports, 15(1). doi:10.1038/s41598-025-90093-1.

[12] Maleki, M., Babaei, E., & Tarafdar Hagh, M. (2025). Hybrid high step-up DC-DC converter based on quadratic and switched capacitor cells with reduced voltage stress across the switches. International Journal of Electronics, 112(7), 1360–1380. doi:10.1080/00207217.2024.2378490.

[13] Hasanpour, S. (2025). A novel soft-switched trans-inverse ultra-high-gain DC/DC converter with low switch voltage stress. Scientific Reports, 15(1). doi:10.1038/s41598-025-17301-w.

[14] Alavi, P., Mohseni, P., Babaei, E., & Marzang, V. (2020). An Ultra-High Step-Up DC–DC Converter with Extendable Voltage Gain and Soft-Switching Capability. IEEE Transactions on Industrial Electronics, 67(11), 9238–9250. doi:10.1109/tie.2019.2952821.

[15] Sadeghpour, D., & Bauman, J. (2022). High-Efficiency Coupled-Inductor Switched-Capacitor Boost Converter with Improved Input Current Ripple. IEEE Transactions on Industrial Electronics, 69(8), 7940–7951. doi:10.1109/TIE.2021.3109505.

[16] Sakthiram, T., Yogesh, L., Srikanth, R., Prabhakar, M., & Angalaeswari, S. (2025). Single-switch ultra-high step-Up DC-DC converter for PV applications. Results in Engineering, 25. doi:10.1016/j.rineng.2025.104050.

[17] Lee, S. S., Chu, B., Lim, C. S., & Lee, K. B. (2019). Two-inductor non-isolated DC-DC converter with high step-up voltage gain. Journal of Power Electronics, 19(5), 1069–1073. doi:10.6113/JPE.2019.19.5.1069.

[18] Rosas-Caro, J. C., Sanchez, V. M., Valdez-Resendiz, J. E., Mayo-Maldonado, J. C., Beltran-Carbajal, F., & Valderrabano-Gonzalez, A. (2018). Quadratic buck-boost converter with positive output-voltage and continuous input-current. 2018 International Conference on Electronics, Communications and Computers (CONIELECOMP), 152–158. doi:10.1109/conielecomp.2018.8327191.

[19] Mizani, A., Shoushtari, M., & Shoulaie, A. (2020). A Novel Quadratic High Step-up DC-DC converter. 2020 11th Power Electronics, Drive Systems, and Technologies Conference, PEDSTC 2020. doi:10.1109/PEDSTC49159.2020.9088469.

[20] Rahimi, T., Islam, M. R., Gholizadeh, H., Mahdizadeh, S., & Afjei, E. (2021). Design and Implementation of a High Step-Up DC-DC Converter Based on the Conventional Boost and Buck-Boost Converters with High Value of the Efficiency Suitable for Renewable Application. Sustainability, 13(19), 10699. doi:10.3390/su131910699.

[21] Zhang, Y., Liu, H., Li, J., Sumner, M., & Xia, C. (2019). DC-DC Boost Converter with a Wide Input Range and High Voltage Gain for Fuel Cell Vehicles. IEEE Transactions on Power Electronics, 34(5), 4100–4111. doi:10.1109/TPEL.2018.2858443.

[22] Valdez-Resendiz, J. E., Rosas-Caro, J. C., Mayo-Maldonado, J. C., & Llamas-Terres, A. (2018). Quadratic boost converter based on stackable switching stages. IET Power Electronics, 11(8), 1373–1381. doi:10.1049/iet-pel.2017.0278.

[23] Gupta, N., Bhaskar, M. S., Almakhles, D., Sanjeevikumar, P., Blaabjerg, F., & Leonowicz, Z. (2020). Two-Tier Converter: A New Structure of High Gain DC-DC Converter with Reduced Voltage Stress. 2020 IEEE International Conference on Environment and Electrical Engineering and 2020 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe), 1–6. doi:10.1109/eeeic/icpseurope49358.2020.9160526.

[24] Totonchi, N., Gholizadeh, H., Afjei, E., & Hamzeh, M. (2020). A Novel Transformer less High Gain DC-DC Converter with Continuous Input Current and Suitable for Photo Voltaic Panels. 2020 11th Power Electronics, Drive Systems, and Technologies Conference, PEDSTC 2020. doi:10.1109/PEDSTC49159.2020.9088497.