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Performance Evolution of Multi-Valued Nano Inverters

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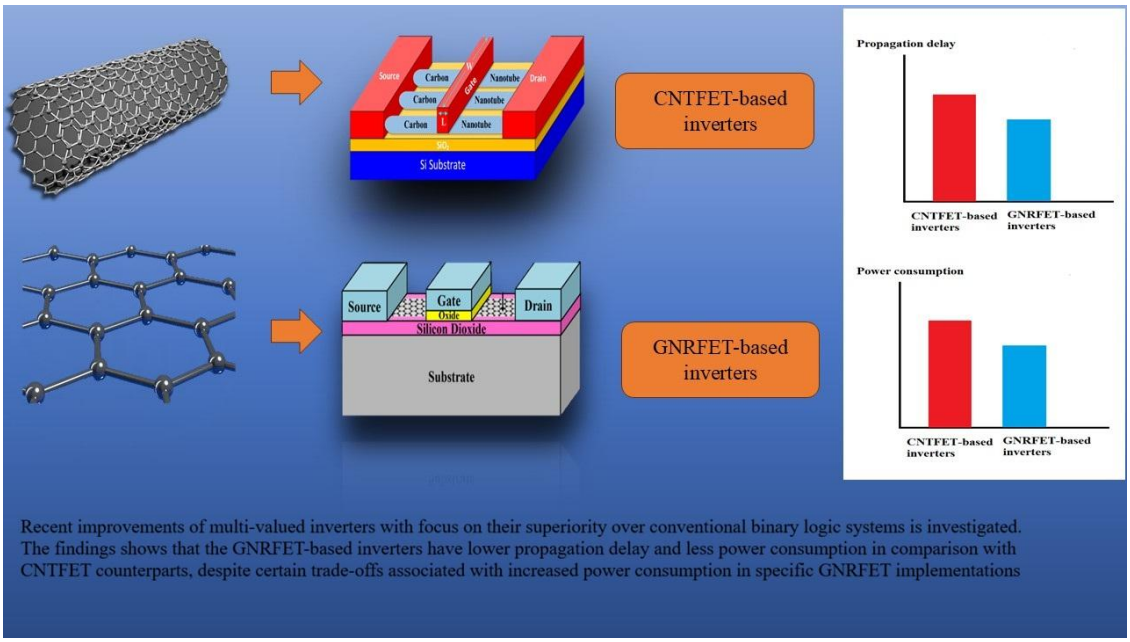
Abstract:

This paper investigates recent improvements in multi-valued inverters, focusing on their superiority over conventional binary logic systems. The main focus is on cutting-edge transistors for logic gates, particularly Carbon Nanotube Field Effect Transistors (CNTFET) and Graphene Nanoribbon Field Effect Transistors (GNRFET). We analyze the structural and operational principles of these emerging transistors by comparatively evaluating their performance across parameters such as PDP, delay, power consumption, and fabrication complexity. This paper focuses on CNTFET- and GNRFET-based ternary and quaternary inverters. To better assess the performance of multi-valued inverters and identify the best candidate, we investigate pentanary and binary inverters. The findings show that GNRFET-based inverters have lower propagation delay and lower power consumption than CNTFET counterparts, despite trade-offs associated with increased power consumption in specific GNRFET implementations.

Graphical Abstract



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1. Introduction

For decades, binary logic has been the most widely used approach to design digital circuits due to its inherent two-state switching mechanism (0 and 1) [1, 2]. By increasing the usage of digital circuits, the computational complexity, and massive data transmission in applications such as Artificial Intelligence (AI) [3], binary logic faces with critical challenges such as high interconnection density on circuits, large silicon area, and limited efficiency in estimation and analysis tasks [2, 4]. Furthermore, although Moore's law predicts the doubling of transistor density approximately every two years, continued lithographic scaling toward atomic dimensions is approaching fundamental physical limits [5]. An alternative method to overcome the limitation of binary logic is implementing Multi-Valued Logic (MVL) in circuit design [6]. In MVL, data transferring is done by multiple logic levels, which provides faster data transfer, reducing transistor count, area reduction, and reducing the number of interconnections [1, 7-10]. Recently, the most widely adopted MVL, which most research has focused on include: Ternary [11], Quaternary [12], and Pentanary [13] and in some cases fuzzy logic [14]. However, only a few studies have investigated pentanary logic. To realize MVL, distinct threshold voltages are required, charge-coupled devices [15], voltage-mode CMOS [16], and current-Mode CMOS [17] are common methods. Among these, voltage-mode CMOS is the most practical technique. However, CMOS is limited by increasing transistor counts on a silicon wafer and scaling challenges such as reducing gate control, increasing power density, lithography costs, large parametric variations, and very high leakage currents [2, 13]. Effective alternatives to address the drawbacks of CMOS and downsizing challenges include QCA [18, 19], Memristor [20], Spintronic devices [21, 22] and novel transistors such as Carbon Nanotube Field Effect Transistors (CNTFETs) [23-25], Graphene Nanoribbon Field Effect Transistors (GNRFETs) [26], Fin Field Effect Transistors (FinFETs) [27], Quantum dot transistors [28] and Single electron transistors [29]. Among these, CNTFETs and GNRFETs are the most extensively investigated technologies because of their extraordinary characteristics, physical attributes, and potential as CMOS alternatives.

Although prior studies have addressed the design and implementation of individual CNTFET-based and GNRFET-based inverters with distinct logic radix, this work provides a comprehensive comparison of both technologies based on their physical attributes to evaluate their suitability as CMOS alternatives. Moreover, by quantitatively analyzing different parameters such as switching speed, implementation complexity, transistor count, and scalability across different logic radices, this study identifies the most suitable technology for efficient multi-valued digital inverter design. It establishes practical design guidelines beyond functional validation.

In the rest of the study, section 2 investigates the structure and physical properties of MOSFET-like CNTFET and GNRFET transistors as background. In section 3, we investigate different designs of CNTFET-based inverters with different logics, from binary to pentanary. In section 4, the wide structures of MVL GNRFET-based inverters are studied. Subsequently, section 5 compares the investigated CNTFET- and GNRFET-based inverters in terms of delay, PDP, and power consumption to identify the superior technology for digital circuits, and section 6 concludes the article.

2. Backgrounds

2.1. CNTFETs

The CNTs, which can be formed as rolled up graphene sheet and are classified to Single Wall CNTs (SWCNTs), and Multi Wall CNTS (MWCNTs) [2]. The SWCNTs are commonly used as the channel in CNTFETs due to their straightforward manufacturing process [30]. In SWCNTs, the carbons atom arrangement is characterized by the chirality vector (n, m), which extremely affects the electronic properties of the nanotube. The CNTs are metallic when n=m or n−m=3i; otherwise, they exhibit semiconducting behavior [1]. Among distinct CNTFET structures, which include Schottky Barrier CNTFETs (SB-CNTFETs) [31], Tunneling CNTFETs (T-CNTFETs) [32] and MOSFET-like CNTFETs [33], the MOSFET-like CNTFET structure is the most investigated due to its compatibility with established fabrication processes [13]. The schematic of a CNTFET is illustrated in Figure 1 [2].

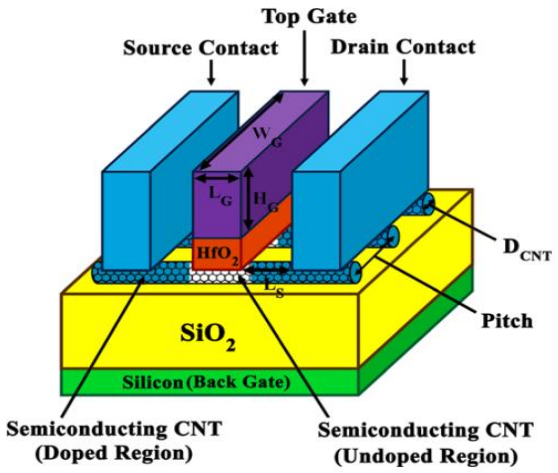

Figure 1. Structure of a CNTFET, which is similar to a MOSFET (Adapted from [2])

2.2. GNRFETs

Graphene is a two-dimensional allotrope of carbon, which demonstrates remarkable electrical properties and is compatible with planar technology [34]. However, its zero-bandgap nature significantly limits its direct application in FETs. To overcome these limitations, Graphene Nanoribbons (GNRs), narrow strips of graphene with nanometer-scale widths, have been proposed as a promising channel material. According to Nayeri et al. [35], when the width is reduced below approximately 10^{nm}, GNRs exhibit semiconducting behavior, and recent fabrication advances have enabled widths below 2^{nm} [37]. Consequently, GNRFET-based devices have become practically feasible [36]. Structurally, GNRs are generally classified into Zigzag GNRs (ZGNRs) and Armchair GNRs (AGNRs). ZGNRs inherently show metallic behavior, whereas AGNRs can be either semiconducting or metallic, depending on their number of dimer lines. AGNRs are semiconducting when m = 3q or 3q + 1, and metallic when m = 3q + 2. The electronic properties of AGNRs, including their bandgap and width dependence, can be described using mathematical equations in Nabi and Rezai [23]. The structure of a GNRFET is shown in Figure 2.

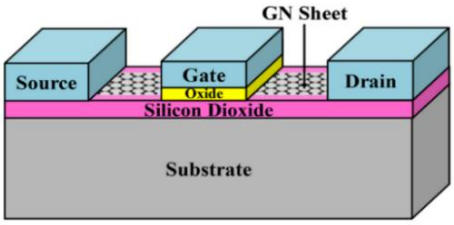

Figure 2. Structure of a GNRFET [34]

3. Methodology

In this study, simulations were performed in HSPICE using the Compact SPICE model for 32^{nm} CNTFET technology and 16^{nm} and 32^{nm} GNRFET technologies.

3.1. CNTFET-based Binary Inverters

In Khandelwal and Sharan [37], the binary and ternary logic inverters were implemented using CNTFET and CMOS at the 32^{nm} technology node, and these two structures were evaluated in terms of performance metrics to determine the most suitable technology for logic circuit design. Figure 3 shows the binary logic CMOS and CNTFET-based inverter. As shown, CMOS and CNTFET-based inverters use 2 transistors (one p-channel and one N-channel); however, the CNTFET-based inverter requires fewer interconnections.

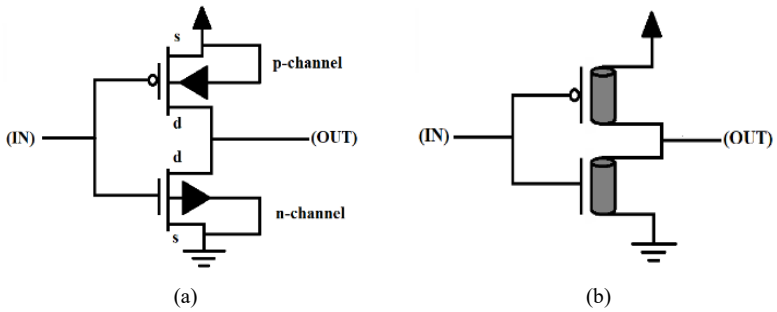

Figure 3. The structure of (a) binary CMOS inverter and (b) binary CNTFET-based inverter in Khandelwal and Sharan [37]

In Singh et al. [38], the binary and ternary logic inverters were implemented using CNTFET and CMOS at the 16^{nm} technology node. In Singh et al. [38], delay, average power and PDP were evaluated for three types of dielectrics. Table 1 provides the performance of the CNTFET and CMOS-based inverters.

Table 1. Delay, average power, and power delay product for both CNTFET and CMOS-based inverters in Singh et al. [38]

Dielectric Material	CMOS			CNTFET		
	Delay (ps)	P_{av} (µW)	PDP (aJ)	Delay (ps)	P_{av} (µW)	PDP (zJ)
SiO2	1.018	34.981	35.615	1.796	0.002125	0.003818

3.2. CNTFET-based Ternary Inverters

In Lin et al. [1], NTI, PTI, and STI were designed and examined. The NTI and PTI implementations relied on CNTFETs with distinct CNT diameters of 1.487^{nm} and 0.783^{nm}. This approach was adopted to achieve different V_{th}. The structure of the proposed NTI and PTI in Lin et al. [1], are shown in Figure 4. The primary difference between the NTI and PTI designs lies in the arrangement of CNTFETs with different chirality's.

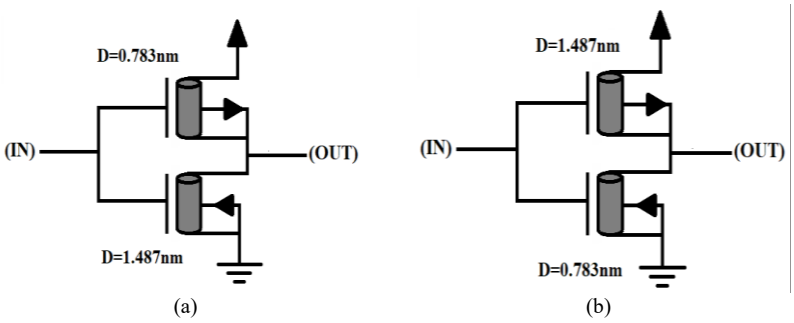

Figure 4. Structure of ternary NTI and PTI in Lin et al. [1]

In Moaiyeri et al. [13], several novel logic circuits were designed using 32^{nm} CNTFET technology and subsequently analyzed through HSPICE simulations. The study also investigated quaternary and pentanary logic circuits, demonstrating the performance and scalability of CNTFET-based circuits for MVL implementation. This section investigates the calculated parameters of the proposed STI. Table 2 presents the results of the ternary inverter implementations. As reported in Moaiyeri et al. [13], ternary logic requires only two distinct CNT diameters, specifically 1.487^{nm} and 0.783^{nm}. The structure of the ternary inverter in Moaiyeri et al. [13] is shown in Figure 5.

Table 2. The performance of STI in Moaiyeri et al. [13]

Inverter type	Delay(ps)	Energy consumption (aJ)	Average power consumption (10^{-7} w)
STI	16.579	3.2151	1.9392

As illustrated in Figure 5, the proposed STI in Moaiyeri et al. [13] is implemented using six CNTFETs with 2 distinct nanotube chiralities.

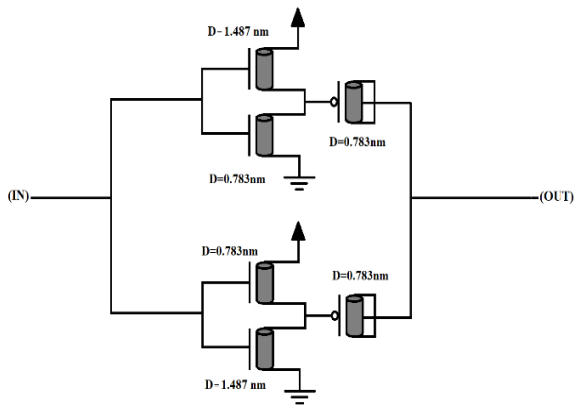

Figure 5. Structure of STI with 2 distinct chirality vectors and 6 transistors in Moaiyeri et al. [13]

In Abbasian et al. [39], ternary logic gates such as TNOR, TNAND, TBUF, and STI were implemented and evaluated based on performance metrics. These logic gates are designed with 32^{nm} technology node. To implement the STI, 10 CNTFETs with three different nanotube chirality's is required. Table 3 presents the STI performance and transistor count.

Table 3. The performance of the proposed STI in Abbasian et al. [39]

	Transistors count	Worst-case delay (ps)	Average power(μW)	PDP (aJ)
STI	6	29	0.091	2.64

In Tabrizchi et al. [4], three-output/state logic CNTFET-based circuits are implemented at 32^{nm}. A key novelty of the proposed circuit's structures is the ability to utilize both a logic function and its complement through a control signal within each logic device. Furthermore, these circuits feature a high-impedance state, which effectively reduces power consumption when the circuit is idle. For the ternary NOT/BUFFER implementation, only two distinct CNT diameters, 0.783^{nm} and 1.478^{nm}, achieve the required threshold-voltage differentiation. Figure 6 illustrates the schematic design of this novel ternary structure, while Table 4 summarizes the corresponding performance metrics, including PDP, power consumption, maximum delay, and propagation delay. In this structure, the transistor count is 10, higher than in other reported designs. However, this configuration integrates both buffer and NOT functionalities within the same logic circuit.

Table 4. Result of proposed Ternary inverter in Tabrizchi et al. [4]

Parameter / gate	Delay (ps)	PDP (aJ)	Power (μW)	Maximum Delay (μs)
Buffer	18.78	33.26	1.7711	18.78
NOT	7.81	33.26	1.7711	18.78

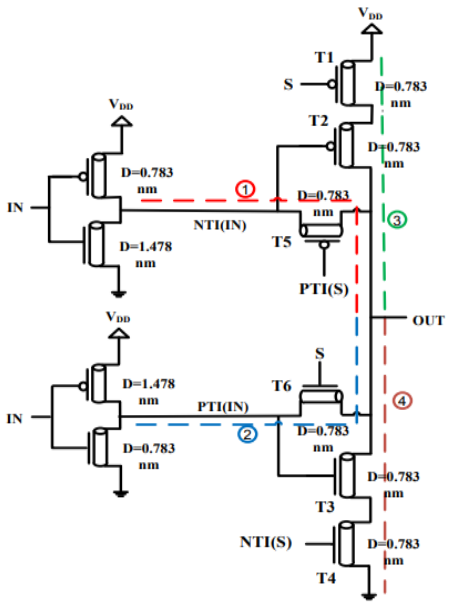

Figure 6. Structure of a buffer/not circuit with 10 transistors in a circuit in Tabrizchi et al. [4]

In Moaiyeri et al. [40], several robust CNTFET-based ternary circuits were proposed. To implement the STI, CNTs with three distinct chirality vectors, namely (19,0), (14,0), and (10,0), were employed. Table 5 summarizes the propagation delay, power consumption, and energy consumption of the proposed cascaded STI. Figure 7 illustrates the schematics of the single STI implemented with both NTI and PTI. These results demonstrate the robustness and efficiency of the proposed CNTFET-based ternary logic structures under realistic physical and electrical constraints.

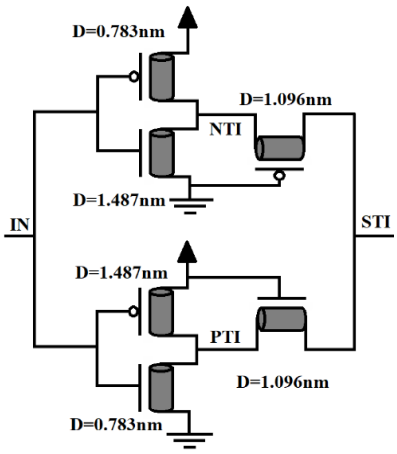

Figure 7. Schematic of STI employed 6 CNTFETs with 3 distinct chirality vectors in Moaiyeri et al. [40]

Table 5. Delay, power, and energy consumption of the proposed cascaded STI with 6 transistors in Moaiyeri et al. [40]

Parameter / V_{DD}	Delay (ps)	Power (μW)	Energy consumption (aJ)
0.8	82.659	0.16399	13.555
0.9	59.088	0.27895	16.482
1	48.425	0.60480	29.287

In Samadi et al. [41], several CNTFET-based ternary logic STIs, such as resistor-loaded and transistor-loaded configurations, are designed and evaluated to determine delay, average power, and PDP. In this study, the ternary STI uses 6 CNTFETs with 2 distinct chirality vectors. The corresponding performance of this STI is presented in Table 6.

Based on the results, the transistor load STI performs much better due to its lower PDP.

In Krishna et al. [42], some ternary arithmetic logic circuits were implemented using the 32^{nm} Stanford CNTFET model in HSPICE. Table 7 provides the evaluated parameters and STI performance metrics. The proposed STI in Krishna et al. [42] is implemented with 6 CNTFETs, 3 different chirality vectors, and distinct CNT diameters.

Table 6. Performance of proposed RES-load and Tr-load in Samadi et al. [41]

Parameter / gate	D_{avg} (ps)	P_{avg} (µW)	PDP (aJ)
Proposed RES-load	0.98833	0.69087	0.68280
Proposed Tr-load	1.0604	0.27581	0.29246

Table 7. Performance of the proposed STI in Krishna et al. [42]

Parameter / gate	delay(ps)	Power Usage (µW)	PDP (aJ)
STI	30980	0.000105	3.253

In RatanKumar et al. [43], some complex circuits such as a full adder and full subtractor are designed using AND, OR, and STI. In [43], the Pseudo N-type CNTFETs are employed to design these logic gates. The structure of the utilized STI in RatanKumar et al. [43] is shown in Figure 8. The results obtained from the STI pseudo are given in Table 8. In RatanKumar et al. [43], in contrast with other studies that implement STIs using 6 CNTFETs, RatanKumar et al. require only 4 CNTFETs (2 n-type and 2 p-type).

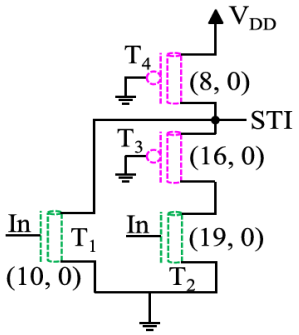

Figure 8. Schematic Pseudo CNTFET-based inverter in RatanKumar et al. [43]

Table 8. Results of pseudo-STI in RatanKumar et al. [43]

Inverter	Delay (ps)	Power Dissipation (µW)	PDP (aJ)
STI pseudo	920	0.77	700
Complementary	5650	4.25	24000

3.3. CNTFET-based Quaternary Inverters

This section explores different structures of CNTFET-based quaternary inverters. The number of studies on quaternary CNTFET circuits is far fewer than those on ternary CNTFET-based circuits.

In Ebrahimi et al. [44], several quaternary logic circuits, including inverters, are designed and implemented, and their performance metrics are evaluated under varying C-load conditions. The quaternary inverters employed 2 to 10 CNTFETs with three chirality vectors (8,0), (13,0), and (29,0) to achieve the required threshold voltages for quaternary logic states. The structural schematics of the proposed SQI, NQI, PQI, and IQI are depicted in Figure 9. The results of these structures are provided in Table 9.

In Moaiyeri et al. [13], the structure of CNTFET-based quaternary NOT (QNOT) is investigated. In this design, three distinct CNT diameters of 2.27^{nm,} 0.783^{nm} and 1.487^{nm} are employed to produce quaternary logic levels. Table 10 summarizes the results. The corresponding structure of the quaternary inverter is shown in Figure 10. To implement this structure, 10 CNTFETs are required

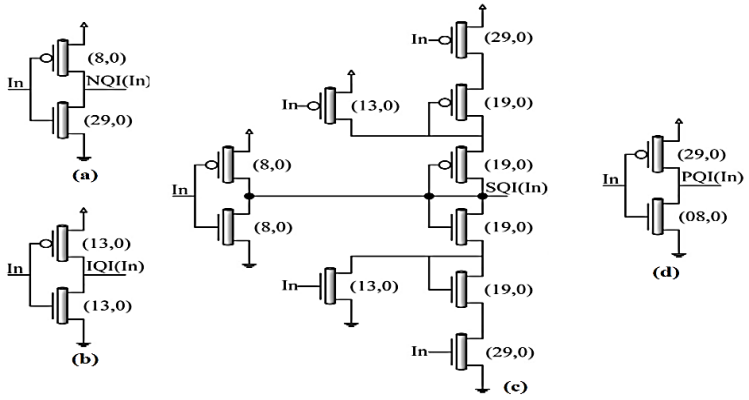

Figure 9. The provided structure of Quaternary (a) NQI, (b) IQI, (c) SQI, and (d) PQI in[44]

Table 9. The metric parameters of quaternary CNTFET-based inverters in Ebrahimi et al. [44]

C-Load	Parameter	NQI	IQI	SQI	PQI
0e-15f	Power (µW)	0.009	0.0131	0.9556	0.0087
	Delay (ps)	1.3	0.91	1.7393	1.2258
	PDP (aJ)	0.012	0.01193	1.6621	0.01067
1e-15f	Power (µW)	0.08	0.0849	0.9958	0.0785
	Delay (ps)	113.5	69.1	39.766	118.44
	PDP (aJ)	9.03	5.8696	39.599	9.2983
2e-15f	Power (µW)	0.19	0.1576	1.0359	0.1493
	Delay (ps)	224.6	132.35	77.668	224.78
	PDP (aJ)	33.3	20.858	80.456	33.56
3e-15f	Power (µW)	0.22	0.2241	1.0758	0.2159
	Delay (ps)	333.1	199.21	116.01	336.5
	PDP (aJ)	73.2	44.643	120.18	72.65
4e-15f	Power (µW)	0.29	0.2978	1.1156	0.2885
	Delay (ps)	444.9	263.55	153.76	443.72
	PDP (aJ)	126	78.485	171.54	128.01
Transistor Count		2	2	10	2

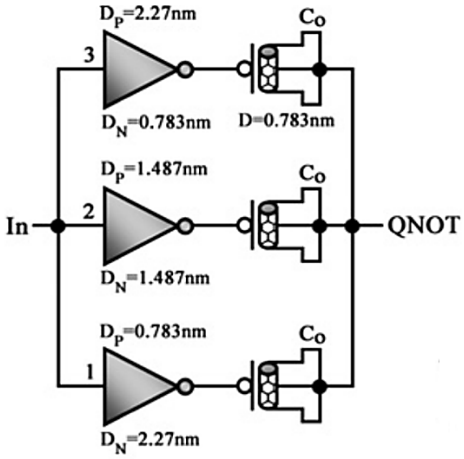

Figure 10. The structure of QNOT in Moaiyeri et al. [13]

Table 10. The results of QNOT in Moaiyeri et al. [13]

V_{DD} \ Parameter	Delay (ps)	Power (µW)	Energy consumption (aJ)
0.8	24.136	0.4593	11.086
0.9	19.067	1.3579	25.892

1	16.912	3.3217	56.176

3.4. CNTFET-based Pentanary Inverters

This section examines pentanary logic circuit structures. Research on radix-5 logic paradigm remains limited compared to lower-radix multi-valued systems.

In Moaiyeri et al. [13], the authors proposed pentanary CNTFET-based circuits. Pentanary logic operates in radix-5, with logic values defined as 0, 1, 2, 3, and 4. In Basha and Venkatramana [34], the radix-5 logic is alternatively referred to as quinary logic. The implementation of CNTFET-based Pentanary NOT (PNOT) employs three different CNT diameters 0.783^{nm}, 1.096^{nm}, and 2.975^{nm} corresponding to four distinct chirality vectors, namely (10, 0), (14, 0), and (38, 0). Figure 11 illustrates the schematic structures of the proposed PNOT. Table 11 presents the results for the proposed PNOT.

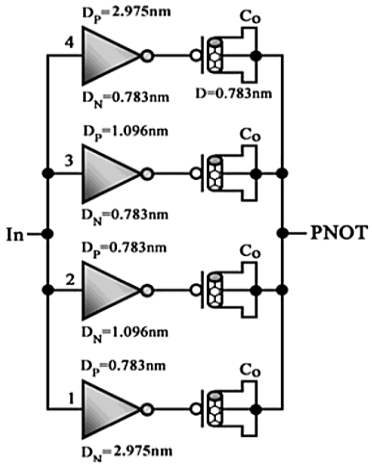

Figure 11. The structure of PNOT in Moaiyeri et al. [13]

Table 11. The results of PNOT in Moaiyeri et al. [13]

V_{DD} \ Parameter	Delay (ps)	Power (µW)	Energy consumption (aJ)
0.8	108.03	0.8876	95.891
0.9	65.126	1.9560	127.39
1	42.353	4.3874	185.82

4. GNRFET-based Inverters

4.1. GNRFET -based Ternary Inverters

In Madhuri and Sunithamani [26], the design of STI, NTI, and PTI is presented. to use the STI, 6 GNRFETs with three different channel widths of 1.59^{nm}, 1.23^{nm}, and 0.86^{nm} are required. The supply voltage (V_{DD}) is set to 0.9^{V}; consequently, logic level 0 corresponds to 0^{V}, logic level 1 corresponds to 0.45^{V}, and logic level 2 corresponds to 0.9^{V}. Figure 12 illustrates the structures and the ternary GRNFET-based inverters. The average propagation delay for the designed STI is 21.03^{ps}.

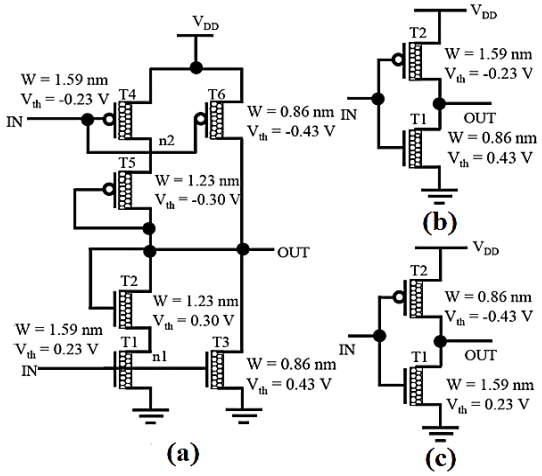

Figure 12. Schematic of (a) STI, (b) PTI, and (c) NTI in Madhuri and Sunithamani [26]

In Sandhie et al. [45], the design of NTI, PTI, and STI and their comparison with other inverters is discussed. These inverters are illustrated in Figure 13 [45]. For NTI, the number of dimmer lines (N) for p-type and n-type GRNFETs is 7 and 9, respectively. For PTI, N for p-type and n-type GNRFETs are 9 and 7, respectively. In Sandhie et al. [45], the width of the local GNR connections between transistors is 20^{nm}, which is significantly shorter than the average free path of graphene, and thus, its resistance can be neglected. Table 12 presents the results obtained from the STI in [45]. Moreover, the designed circuit is depicted in Figure 13.

Table 12. The result of the STI in Sandhie et al. [45]

Logic Gates	Transistor count	Delay (ps)	Total power (µW)	PDP (aJ)
STI	6	11	88.6	0.98

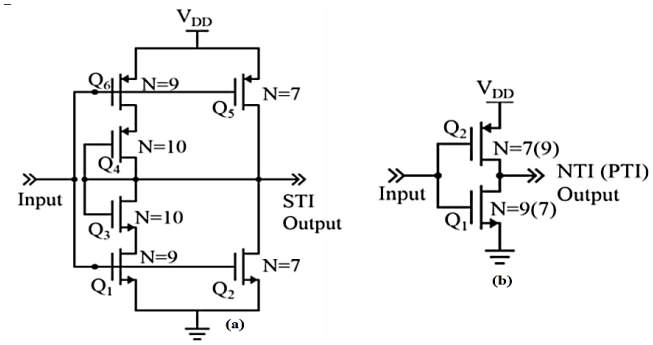

Figure 13. The structure of (a) STI and (b) NTI in Sandhie et al. [45]

The obtained results from the STI inverter are presented in Table 12.

In Mahesh and Shameem [46], ternary inverters are designed and utilized. In this paper, NTI and PTI are designed, and the STI is produced by combining these inverters. These structures are shown in Figure 14 [46].

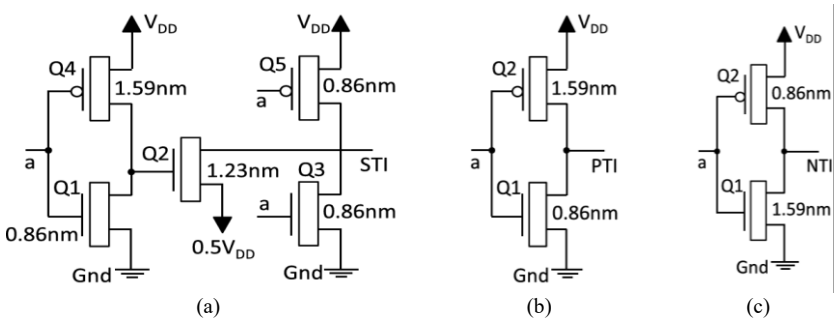

Figure 14. The structure of (a)STI, (b) PTI, and (c)NTI [46]

Table 13 shows the results of the proposed inverters in Mahesh and Shameem [46].

Table 13. The results of the proposed inverters in Mahesh and Shameem [46]

	Delay (ps)		
V_{DD}	0.8V	0.9V	1V
STI	0.06298	0.05824	0.05523
NTI	0.0357	0.0284	0.0167
PTI	0.0276	0.00157	0.00101
	Power (µw)		
STI	10.78	13.46	18.45
NTI	2.01	4.12	6.56
PTI	1.98	3.44	5.98

4.2. Quaternary GNRFET-based Inverters

In Basha and Venkatramana[34] designed and implemented the structure of quaternary GNRFET-based logic circuits. They used GNRFET-based SQI, IQI, PQI, and NQI and measured and compared their propagation delay, power dissipation, and PDP with CNTFET-based inverters. To design the SQI, ten GNRFETs with diameters of 0.86^{nm}, 0.98^{nm}, 1.23^{nm}, and 1.97^{nm}

are used. These GRN widths produce threshold voltages of 0.43^{V}, 0.56^{V}, 0.30^{V}, and 0.19^{V}. Figure 15 shows the inverter structure, and Table 14 presents the results.

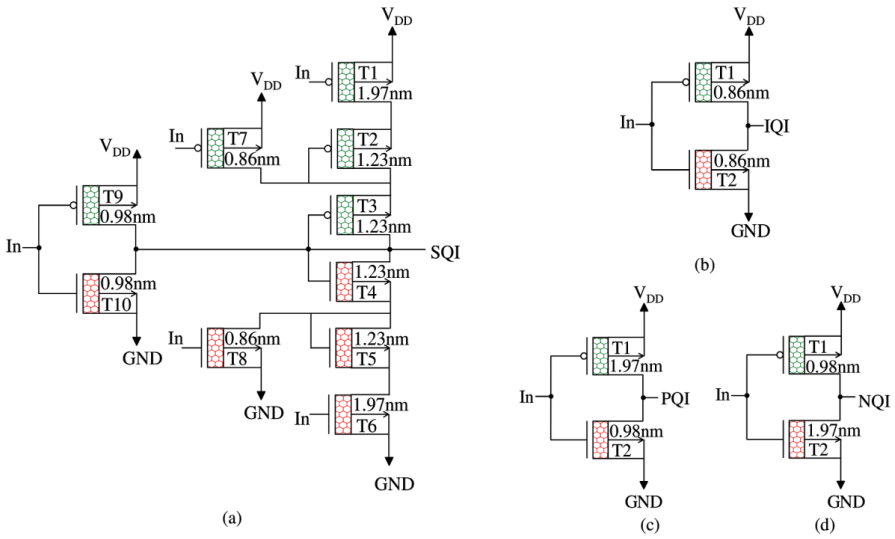

Figure 15. The structure of (a) SQI, (b) IQI, (c) PQI, and (d) NQI [34]

Table 14. The result of quaternary inverters in Basha and Venkatramana [34]

Parameters	SQI	IQI	NQI	PQI
propagation delay (ps)	7.54	2.52	2.53	2.52
Power Dissipation (μW)	0.48	0.24	0.88	0.40
Power Delay Product (aJ)	3.6	٠.6	2.2	1.0

5. Results

5.1. Physical and Electrical Properties of CNTs and GRNs

This section investigates the intrinsic properties of CNTs and GNRs to identify the best choice for designing and implementing future transistors. Both CNTs and GNRs show interesting characteristics, which makes them suitable for designing semiconducting devices. Some of these characterizations are provided in Table 15 [26].

Table 15. Physical and electrical attributes of CNTs and GNRs [26]

Properties	CNTs	GRNs
thermal conductivity, W/mK	3000	5000
mobility, $cm^2 \cdot V^{-1} \cdot s^{-1}$	1,00,000	2,00,000
electrical conductivity, $S \cdot cm^{-1}$	5000	10^6
density, $g \cdot cm^{-3}$	1.33	>1.0
fracture strength, GPa	45	124

Based on our investigation, the GNRs are superior to CNTs in all terms. Moreover, according to Majumder al. [47], GNRs have much lower defects, resulting in better electrical properties and improved electrical transfer. Furthermore, a new method of GNR production has recently been achieved, which enables GNRs to be produced with sizes less than 2^{nm}. This new production method, and technical limitations in the production of CNTs, force the semiconductor industry to sooner or later design novel devices based on GNRs [48].

5.2. Complexity of the MVL Circuits

In this section, the structural configurations of binary, ternary, quaternary, and pentanary CNTFETs and GNRFET-based inverters are analyzed and then compared. The analysis focuses on circuit topologies and transistor counts. Both CNTFETs and CMOS use only 2 transistors for binary inverters. Whereas ternary inverters, in CMOS, CNTFET, and GNRFET, require between 2 and 6 transistors [7, 26, 27, 37, 46, 49]. Based on Figure 4, using a CMOS implementation of voltage-mode MVL increases interconnection count and the complexity of digital circuits. While MVL reduces interconnect complexity at the system level by decreasing the number of signal lines required for information representation, higher-radix inverters require more transistors and more sophisticated circuit topologies. Therefore, achieving an optimal balance between logic radix, transistor count, and structural complexity remains a critical design challenge in CNTFET- based and GNRFET-based MVL circuits. For higher-radix implementations, the increase in transistor count becomes more pronounced. Based on Dan and

Mahapatra [29] and Basha and Venkatramana [34], a GNRFET-based quaternary SQI requires 10 GNRFETs. Moreover, according to Moaiyeri et al. [2], quaternary and pentanary inverters require more transistors than ternary and binary inverters.

5.3. Comparison of MOSFET-, CNTFET-, and GRNFET-based Circuits

In this section, metric parameters of CNTFET-, GNRFET-, and MOSFET-based STI in different logic are summarized and compared to identify the best structure for implementation. Table 16 presents the summarized results of this comparative analysis. Based on the quantitative data in Table 16, a clear technology-dependent trend in PDP across different logic radices is evident. For binary logic, the PDP of CNTFET-based inverters [38] (3.818×10^{-21}J) is nearly 9300 times lower than that of MOSFET counterparts [38] (35.615×10^{-18}J), which indicates a substantial energy advantage at binary logic. In ternary logic, the minimum reported PDP values reach 0.68×10^{-18}J [41] for CNTFET and 0.395×10^{-18}J [35] for GNRFET structures, while MOSFET-based ternary designs remain in the range of 24–34.9×10^{-18}J. This indicates that, at radix-3, GNRFET achieves approximately 2.3 times lower PDP than the best CNTFET design, and nearly two orders of magnitude improvement over CMOS implementations. However, CNTFET-based ternary circuits exhibit wide PDP dispersion, ranging from 0.2946×10^{-18} J to 700×10^{-18} J, indicating strong dependence on topology and chirality engineering.

Table 16. Comparison over CNTFET,GNRFET, MOSFET

PDP (aJ)		
CNTFET	**GNRFET**	**MOSFET**
Binary logic		
3.818×10^{-3}[38]	-	35.615[38]
Ternary logic		
3.214[13]	0.302 [45]	
2.64[39]		
33.26[4]	24.2[27]	
29.287[40]	34.9	
0.2946[41]	0.395[35]	
3.25[42]	4.19[49]	
700[43]	1.3 [50]	
Quaternary logic		
1.66[44]	3.6[34]	1590.63[2]
10.86[13]		
92.033[2]		
Pentanary logic		
185.82[13]		
Delay (ps)		
Binary logic		
CNTFET	**GNRFET**	**MOSFET**
1.796 [38]		1.018[38]
Ternary logic		
16.579[13]	13 [45]	
29 [39]	55230[46]	
7.81 [4]	29.95 [27]	
48.425 [40]	1.57 [51]	
1.0604[41]	1.8 [35]	
30980 [42]	0.38 [49]	
920 [43]	11.2 [50]	
Quaternary logic		
1.7393[44]	7.54[34]	33.071[2]
16.912[13]		
2.9412[2]		
Pentanary logic		
42.353[13]		
Power (µw)		
Binary logic		

CNTFET	GNRFET	MOSFET
0.002125 [38]		34.981[38]
Ternary logic		
0.1939 [13]	0.02322 [45]	
0.091 [39]	18.45 [46]	
0.9556[4]	8.172 [27]	
0.6048 [40]	22.2 [51]	
0.27581 [41]	0.23[35]	
0.000105[42]	11.042[49]	
0.77 [43]	0.117[50]	
Quaternary logic		
0.9556[44]	0.48 [34]	48.099[2]
3.3217[13]		
31.588 [2]		
Pentanary logic		
4.3874		

In quaternary logic, the best reported PDP for GNRFET is 0.302×10^{-18} J, which remains lower than 1.66×10^{-18} J for CNTFET based inverter, while MOSFET implementations rise sharply to 1590.63×10^{-18} J. This scaling behavior confirms that energy efficiency significantly reduces with radix in CMOS, moderately in CNTFET, and more gracefully in GNRFET technologies.

In terms of delay, the comparison reveals a more nuanced behavior. In binary logic, MOSFET exhibits a slightly lower delay (1.018^{ps}) compared to CNTFET (1.796^{ps}), suggesting that conventional CMOS remains competitive at radix-2. However, in ternary logic, CNTFET shows a delay as low as 1.0604^{ps}, whereas GNRFET implementations report values ranging from 0.38^{ps} to several nanoseconds, indicating high design sensitivity. The minimum reported GNRFET delay (0.38^{ps}) is approximately 2.8 times faster than the best CNTFET ternary design. Yet, other GNRFET realizations show substantially higher delays, revealing variability driven by ribbon width and device configuration. In quaternary logic, CNTFET achieves 1.7393^{ps} compared to 7.54^{ps} for GNRFET and 33.071^{ps} for MOSFET, indicating that CNTFET provides nearly 4.3 times faster operation than GNRFET and about 19 times faster performance than CMOS at radix-4. Therefore, while GNRFET often achieves the lowest delay under optimized conditions, CNTFET shows more consistently low delay in higher-radix implementations.

In ternary logic, CNTFET power values range from as low as 0.000105$^{\mu W}$ up to 0.6048$^{\mu W}$, whereas GNRFET reports values such as 0. 23$^{\mu W}$ and 22.2$^{\mu W}$, and MOSFET-based implementations rise to 34.981$^{\mu W}$ and 48.099$^{\mu W}$. This implies that optimized CNTFET ternary designs can achieve over 200 times lower power consumption compared to CMOS, while GNRFET achieves approximately 100–300 times reduction depending on topology. In quaternary logic, GNRFET (0.48$^{\mu W}$) consumes roughly half the power of CNTFET (0.9556$^{\mu W}$), whereas MOSFET requires 48.099$^{\mu W}$, nearly 100 times higher than GNRFET.

However, as the radix increases to pentanary, CNTFET exhibits a sharp PDP increase to 185.82×10^{-18} J and delay of 42.353^{ps}, indicating non-linear scaling overhead. Collectively, the numerical evidence suggests that GNRFET offers superior energy efficiency and better PDP scalability for higher-radix MVL. At the same time, CNTFET provides stronger and more consistent delay performance, particularly in quaternary structures. Consequently, GNRFET is more suitable for ultra-low-power MVL systems, whereas CNTFET remains advantageous for high-speed MVL circuit design. Moreover, based on Basha and Venkatramana [34], the proposed GNRFET-based design shows much better performance compared with the similar CNTFET-based design. Table 17 provides this comparison.

Based on Table 17, GNRFET-based inverters perform much better in all terms than CNTFET-based inverters.

Table 17. Comparison between GRNFET and CNTFET-based inverters [34]

GRNFET				
Parameters	SQI	IQI	NQI	PQI
Propagation Delay (ps)	7.54	2.52	2.53	2.52
Power Dissipation (μW)	0.48	0.24	0.88	0.40
Power Delay Product (aJ)	3.6	0.6	2.2	1.0
CNTFET				
Parameters	SQI	IQI	NQI	PQI
Propagation Delay (ps)	11.67	5.09	5.24	5.24
Power Dissipation (μW)	0.72	0.43	0.72	0.39
Power delay Product (aJ)	8.4	2.1	3.7	2.0

5.4. Comparison Functionality of Different Logics

Based on the numerical data reported in Table 16, this section presents the relationship between circuit parameters, logic radix, and clear scaling behavior, which differs significantly among CNTFET, GNRFET, and MOSFET technologies. In terms of PDP, CMOS-based implementations exhibit a strong monotonic degradation as radix increases. While binary CMOS shows 35.615×10^{-18} quaternary rises sharply to 1590.63×10^{-18} J, representing approximately 44.64 times increase from binary to quaternary. This trend reflects the intrinsic overhead of generating and stabilizing multiple voltage levels using conventional transistor networks. In contrast, CNTFET demonstrates a more topology-dependent scaling. Although optimized ternary designs reach as low as 0.68×10^{-18} J, quaternary increases to 1.66×10^{-18} J, corresponding to 2.44 times increase with radix escalation, and pentanary reaches 185.82×10^{-18} J, indicating a dramatic super-linear growth. GNRFET, however, shows a more controlled progression from 0.395×10^{-18}J in ternary to 3.6×10^{-18}J in quaternary, approximately 9 times increase, suggesting better PDP scalability with increasing logic levels.

The delay behavior as a function of radix further clarifies the structural implications of MVL. For CNTFET, delay increases from 1.796^{ps} in binary to 16.579^{ps} in ternary, nearly 9.2 times rise, reflecting the additional intermediate switching states. In quaternary logic, the best reported CNTFET delay is 1.7393^{ps}, which is comparable to binary performance, indicating that topology optimization can mitigate radix-induced delay penalties. However, pentanary delay increases to 42.353^{ps}, approximately 24 times higher than binary, confirming that high-radix scaling introduces substantial propagation overhead. GNRFET shows more moderate delay escalation in quaternary logic (7.54^{ps}) than in ternary optimized values (as low as 0.38ps), representing a worst-case increase of nearly 20 times, depending on design conditions. CMOS, in contrast, demonstrates severe delay inflation at higher radices, reaching 33.071^{ps} in quaternary logic, which is more than 32 times larger than its binary delay (1.018^{ps}). Therefore, delay scaling in CMOS-based inverters is directly affected by logic radix: as the logic radix increases, the delay increases too, whereas CNTFET delay is topology-sensitive and comparatively more stable in optimized GNRFET designs.

Power consumption follows a similar radix-dependent amplification. In CNTFET ternary logic, power can be reduced to 0.000105$^{\mu W}$ under optimized configurations, but increases to 0.9556$^{\mu W}$ in quaternary and 4.3874$^{\mu W}$ in pentanary, corresponding to nearly 41000 times increase from the minimum ternary value to pentanary. This indicates that ultra-low-power operation is highly sensitive to radix expansion. GNRFET shows 0.023$^{\mu W}$ in ternary and 0.48$^{\mu W}$ in quaternary, representing roughly a 5–20 times increase, which remains significantly lower than CMOS quaternary power (35.16$^{\mu W}$), approximately 65 times higher than GNRFET.

Overall, the numerical analysis demonstrates that increasing logic radix inherently amplifies PDP, delay, and power due to additional intermediate voltage states and switching paths. However, the rate of degradation differs by technology: CMOS shows the steepest scaling penalty, CNTFET shows high performance but strong variability and super-linear growth at very high radix. In contrast, GNRFET shows the most balanced and predictable scaling behavior. These results indicate that GNRFET is structurally more suitable for higher-radix MVL implementations, whereas CNTFET is preferable when prioritizing speed in moderate-radix designs.

6. Conclusion

This study presented a comprehensive structural and performance-oriented comparison of binary and MVL CNTFET-based and GNRFET- based inverters. The analysis showed that while binary inverters in both CMOS and CNTFET technologies require only 2 transistors, moving to higher logic radices significantly increases circuit complexity. Specifically, ternary inverters require 4 to 6 transistors, whereas quaternary and pentanary implementations demand higher transistor counts, sometimes reaching 8 to 12 transistors depending on circuit topology. This structural growth directly increases interconnections and biasing requirements. The results clearly indicate that complexity growth is not linear with logic radix; rather, it accelerates because multiple distinct threshold voltages are required.

In terms of performance, quantitative evaluation of delay, average power consumption, and PDP reveals a critical trade-off between logic density and energy efficiency. Although higher-radix logic reduces interconnect density at the system level, the device-level metrics show that propagation delay increases due to cascaded threshold switching and additional transistor stacking. Power consumption also rises as the number of conduction paths grows and intermediate logic states introduce static current components. Consequently, PDP increases with logic radix, indicating reduced energy efficiency per switching event. In structures employing three distinct chirality vectors for CNTFET implementation, more precise threshold-voltage control improves logic stability; however, this advantage comes with increased fabrication sensitivity and slightly higher delay dispersion.

Overall, the comparative investigation indicates that CNTFET-based ternary inverters provide the most balanced trade-off between circuit complexity, controllability of threshold voltages, and energy efficiency. While GNRFET structures exhibit promising electrical characteristics, their dependence on precise nanoribbon width control introduces fabrication variability that may affect threshold uniformity in MVL applications. CNTFET-based STI structures, particularly those using two optimized nanotube diameters, achieve lower PDP and more stable switching behavior than higher-radix alternatives. Therefore, based on structural scalability, quantitative performance metrics, and threshold engineering feasibility, ternary CNTFET-based inverter architectures represent the most practical and energy-efficient solution among the investigated MVL implementations.

7. Statements & Declarations

7.1. Author Contributions

Conceptualization, S.Nabi and A. Rezai; methodology, S.Nabi and A. Rezai; validation, S.Nabi and A. Rezai; formal analysis, S.Nabi and A. Rezai; investigation, S.Nabi and A. Rezai; resources, S.Nabi and A. Rezai; writing—original draft preparation, S.Nabi; writing—review and editing, A. Rezai; visualization, S.Nabi and A. Rezai; supervision, A. Rezai.; project. All authors have read and agreed to the published version of the manuscript.

7.2. Data Availability Statement

Data sharing not applicable: No new data were created or analyzed in this study. Data sharing does not apply to this article.

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There is no funding.

7.4. Declaration of Generative AI and AI-assisted Technologies in the Writing Process

The author(s) declare that no generative AI or AI-assisted technologies were used in the preparation of this manuscript.

7.5. Ethics Approval

Not applicable.

7.6. Informed Consent

Not applicable.

7.7. Consent for Publication

The authors consent to the publication of this manuscript.

7.8. Conflicts of Interest

The authors declare no conflict of interest.

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